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The Future of Reduced Instruction Set Computing and Complex Instruction Set Computing and Suggestions for Reduced Instruction Set Computing-V Development

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Abstract : Based on the two instruction sets of complex instruction set computing (CISC) and reduced instruction set computing (RISC), processors developed in their respective “expertise” fields. This paper will summarize research on the differences in performance and energy efficiency between CISC and RISC and strive to eliminate the influence of peripheral configuration factors. We will discuss whether processor performance is centered around instruction sets or implementation. In addition, the rapidly developing RISC-V poses a challenge to existing models. We will analyze research results, analyze the impact of instruction sets themselves, and finally make suggestions for the development of RISC-V.

Keywords : ISA, RISC-V, ARM, X86, power, energy efficiency
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