World Academy of Science, Engineering and Technology
International Journal of Materials and Metallurgical Engineering
Vol:9, No:05, 2015

Leakage Current Analysis of FinFET Based 7T SRAM at 32nm Technology

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Abstract : FinFETs can be a replacement for bulk-CMOS transistors in many different designs. Its low leakage/standby power property makes FinFETs a desirable option for memory sub-systems. Memory modules are widely used in most digital and computer systems. Leakage power is very important in memory cells since most memory applications access only one or very few memory rows at a given time. As technology scales down, the importance of leakage current and power analysis for memory design is increasing. In this paper, we discover an option for low power interconnect synthesis at the 32nm node and beyond, using Fin-type Field-Effect Transistors (FinFETs) which are a promising substitute for bulk CMOS at the considered gate lengths. We consider a mechanism for improving FinFETs efficiency, called variable supply voltage schemes. In this paper, we've illustrated the design and implementation of FinFET based 4x4 SRAM cell array by means of one bit 7T SRAM. FinFET based 7T SRAM has been designed and analysis have been carried out for leakage current, dynamic power and delay. For the validation of our design approach, the output of FinFET SRAM array have been compared with standard CMOS SRAM and significant improvements are obtained in proposed model.

Keywords : FinFET, 7T SRAM cell, leakage current, delay
Conference Title : ICMN 2015 : International Conference on Microelectronics and Nanotechnology
Conference Location : Berlin, Germany
Conference Dates : May 21-22, 2015