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Implementation of a Baseline RISC for the Realization of a Dynamically Reconfigurable Processor

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Abstract : Reduced instruction set computer (RISC) processors are widely used because of their multiple advantages. In fact, they are based on a simple instruction set so that they increase the speed of the processor and reduce its energy consumption. In this paper, we will present a basic RISC architecture processor that will be developed later to converge to a new architecture with runtime reconfiguration.

Keywords : processor, RISC, DLX, pipeline, runtime reconfiguration
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