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Design of a 28-nm CMOS 2.9-64.9-GHz Broadband Distributed Amplifier with Floating Ground CPW

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Abstract : In this paper, a 1-stage 6-section conventional distributed amplifier (CDA) structure distributed power amplifier (DPA) fabricated in a 28-nm HPC+ 1P9M CMOS process is proposed. The transistor size selection is introduced to achieve broadband power matching and thus remains a high flatness output power and power added efficiency (PAE) within the bandwidth. With the inductive peaking technique, the high-frequency pole appears and the high-frequency gain is increased; the gain flatness becomes better as well. The inductive elements used to form an artificial transmission line are built up with a floating ground coplanar waveguide plane (CPWFG) rather than a microstrip line, coplanar waveguide (CPW), or spiral inductor to get better performance. The DPA achieves 12.6 dB peak gain at 52.5 GHz with 2.9 to 64.9 GHz 3-dB bandwidth. The Psat is 11.4 dBm with PAEMAX of 10.6 % at 25 GHz. The output 1-dB compression point power is 9.8 dBm.

Keywords : distributed power amplifier (DPA), gain bandwidth (GBW), floating ground CPW, inductive peaking, 28-nm, CMOS, 5G.
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