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Transient Enhanced LDO Voltage Regulator with Improved Feed Forward Path Compensation

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Abstract : An ultra low power capacitor less low-dropout voltage regulator with improved transient response using gain enhanced feed forward path compensation is presented in this paper. It is based on a cascade of a voltage amplifier and a transconductor stage in the feed forward path with regular error amplifier to form a composite gain-enhanced feed forward stage. It broadens the gain bandwidth and thus improves the transient response without substantial increase in power consumption. The proposed LDO, designed for a maximum output current of 100 mA in UMC 180 nm, requires a quiescent current of 69 µA. An undershoot of 153.79mV for a load current changes from 0mA to 100mA and an overshoot of 196.24mV for current change of 100mA to 0mA. The settling time is approximately 1.1 µs for the output voltage undershoot case. The load regulation is of 2.77 µV/mA at load current of 100mA. Reference voltage is generated by using an accurate band gap reference circuit of 0.8V.The costly features of SOC such as total chip area and power consumption is drastically reduced by the use of only a total compensation capacitance of 6pF while consuming power consumption of 0.096 mW.

Keywords : capacitor-less LDO, frequency compensation, transient response, latch, self-biased differential amplifier
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