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Application of Carbon Nanotube and Nanowire FET Devices in Future VLSI

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Abstract : The MOSFET has been the main building block in high performance and low power VLSI chips for the last several decades. Device scaling is fundamental to technological advancements, which allows more devices to be integrated on a single die providing greater functionality per chip. Ultimately, the goal of scaling is to build an individual transistor that is smaller, faster, cheaper, and consumes less power. Scaling continued following Moore's law initially and now we see an exponential growth in today's nano scaled chip. However, device scaling to deep nano meter regime leads to exponential increase in leakage currents and excessive heat generation. Moreover, fabrication process variability causing a limitation to further scaling. Researchers believe that with a mix of chemistry, physics, and engineering, nano electronics may provide a solution to increasing fabrication costs and may allow integrated circuits to be scaled beyond the limits of the modern transistor. Carbon nano tube (CNT) and nano wires (NW) based FETs have been analyzed and characterized in laboratory and also been demonstrated as prototypes. This work presents an extensive simulation based study and analysis of CNTFET and NW-FET devices and comparison of the results with conventional MOSFET. From this study, we can conclude that these devices have got some excellent properties and favorable characteristics which will definitely lead the future semiconductor devices in post silicon era.

Keywords : carbon nanotube, nanowire FET, low power, nanoscaled devices, VLSI
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