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Design and Implementation of Wave-Pipelined Circuit Using Reconfigurable Technique

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Abstract : For design of high speed digital circuit wave pipeline is the best approach this can be operated at higher operating frequencies by adjusting clock periods and skews so as latch the o/p of combinational logic circuit at the stable period. In this paper, there are two methods are proposed in automation task one is BIST (Built in self test) and second method is Reconfigurable technique. For the above two approaches dedicated AND gate (multiplier) by applying wave pipeline technique. BIST approach is implemented by Xilinx Spartan-II device. In reconfigurable technique done by ASIC. From the results, wave pipeline circuits are faster than nonpipeline circuit and area, power dissipation are reduced by reconfigurable technique.

Keywords : SOC, wave-pipelining, FPGA, self-testing, reconfigurable, ASIC
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