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A Low Power and High-Speed Conditional-Precharge Sense Amplifier Based Flip-Flop Using Single Ended Latch

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Abstract : This paper presents a low power, high speed, sense-amplifier based flip-flop (SAFF). The flip-flop's power consumption and delay are greatly reduced by employing a new conditionally precharge sense-amplifier stage and a single-ended latch stage. Glitch-free and contention-free latch operation is achieved by using a conditional cut-off strategy. The design uses fewer transistors, has a lower clock load, and has a simple structure, all of which contribute to a near-zero setup time. When compared to previous flip-flop structures proposed for similar input/output conditions, this design's performance and overall PDP have improved. The post layout simulation of the circuit uses 2.91μW of power and has a delay of 65.82 ps. Overall, the power-delay product has seen some enhancements. Cadence Virtuoso Designing tool with CMOS 90nm technology are used for all designs.

Keywords : high-speed, low-power, flip-flop, sense-amplifier
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