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Reconfigurable Efficient IIR Filter Design Using MAC Algorithm

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Abstract : In this paper an IIR filter has been designed and simulated on an FPGA. The implementation is based on MAC algorithm which uses multiply-and-accumulate operations IIR filter design implementation. Parallel Pipelined structure is used to implement the proposed IIR Filter taking optimal advantage of the look up table of the FPGA device. The designed filter has been synthesized on DSP slice based FPGA to perform multiplier function of MAC unit. The DSP slices are useful to enhance the speed performance. The developed IIR filter is designed and simulated with MATLAB and synthesized with Xilinx Synthesis Tool (XST), and implemented on Virtex 5 and Spartan 3 ADSP FPGA devices. The IIR filter implemented on Virtex 5 FPGA can operate at an estimated frequency of 81.5 MHz as compared to 40.5 MHz in case of Spartan 3 ADSP FPGA. The Virtex 5 based implementation also consumes less slices and slice flip flops of target FPGA in comparison to Spartan 3 ADSP based implementation to provide cost effective solution for signal processing applications.

Keywords : butterworth, DSP, IIR, MAC, FPGA
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