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Scheduling Tasks in Embedded Systems Based on NoC Architecture

Authors : D. Dorota

Abstract : This paper presents a method to generate and schedule task in the architecture of embedded systems based on the simulated annealing. This method takes into account the attribute of divisibility of tasks. A proposal represents the process in the form of trees. Despite the fact that the architecture of Network-on-Chip (NoC) is an interesting alternative to a bus architecture based on multi-processors systems, it requires a lot of work that ensures the optimization of communication. This paper proposes an effective approach to generate dedicated NoC topology solving communication problems. Network NoC is generated taking into account the energy consumption and resource issues. Ultimately generated is minimal, dedicated NoC topology. The proposed solution is assumed to be a simple router design and the minimum number of lines.

Keywords : Network-on-Chip, NoC-based embedded systems, scheduling task in embedded systems, simulated annealing
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