World Academy of Science, Engineering and Technology
International Journal of Electronics and Communication Engineering
Vol:14, No:12, 2020

Design and Characterization of a CMOS Process Sensor Utilizing Vth Extractor Circuit

Authors : Rohana Musa, Yuzman Yusoff, Chia Chieu Yin, Hanif Che Lah

Abstract : This paper presents the design and characterization of a low power Complementary Metal Oxide Semiconductor (CMOS) process sensor. The design is targeted for implementation using Silterra’s 180 nm CMOS process technology. The proposed process sensor employs a voltage threshold (V_{th}) extractor architecture for detection of variations in the fabrication process. The process sensor generates output voltages in the range of 401 mV (fast-fast corner) to 443 mV (slow-slow corner) at nominal condition. The power dissipation for this process sensor is 6.3 µW with a supply voltage of 1.8V with a silicon area of 190 µm X 60 µm. The preliminary result of this process sensor that was fabricated indicates a close resemblance between test and simulated results.

Keywords : CMOS process sensor, PVT sensor, threshold extractor circuit, Vth extractor circuit
Conference Title : ICECDS 2020 : International Conference on Electronics, Circuits, Devices and Systems
Conference Location : Kuala Lumpur, Malaysia
Conference Dates : December 17-18, 2020