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The Methodology of Flip Chip Using Astro Place and Route Tool

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Abstract : This paper will discuss flip chip methodology, in which I/O pads, standard cells, macros and bump cells array are placed in the floorplan, then routed using Astro place and route tool. Final DRC and LVS checking is done using Calibre verification tool. The design vehicle to run this methodology is an OpenRISC design targeted to Silterra 0.18 micrometer technology with 6 metal layers for routing. Astro has extensive support for flip chip placement and routing. Astro tool commands for flip chip are straightforward approach like the conventional standard wire bond packaging. However since we do not have flip chip commands in our Astro tool, no LEF file for bump cell and no LEF file for flip chip I/O pad, we create our own methodology to prepare for future flip chip tapeout.

Keywords : methodology, flip chip, bump cell, LEF, astro, calibre, SCHEME, TCL
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