

Performance Analysis of BPJLT with Different Gate and Spacer Materials

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Abstract : The paper presents a simulation study of the electrical characteristic of Bulk Planar Junctionless Transistor (BPJLT) using spacer. The BPJLT is a transistor without any PN junctions in the vertical direction. It is a gate controlled variable resistor. The characteristics of BPJLT are analyzed by varying the oxide material under the gate. It can be shown from the simulation that an ideal subthreshold slope of ~60 mV/decade can be achieved by using highk dielectric. The effects of variation of spacer length and material on the electrical characteristic of BPJLT are also investigated in the paper. The ION / IOFF ratio improvement is of the order of 10⁷ and the OFF current reduction of 10⁻⁴ is obtained by using gate dielectric of HfO₂ instead of SiO₂.

Keywords : spacer, BPJLT, high-k, double gate

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