World Academy of Science, Engineering and Technology
International Journal of Electrical and Computer Engineering
Vol:8, No:07, 2014

# Performance Analysis of BPJLT with Different Gate and Spacer Materials

**Authors :** Porag Jyoti Ligira, Gargi Khanna

**Abstract :** The paper presents a simulation study of the electrical characteristic of Bulk Planar Junctionless Transistor (BPJLT) using spacer. The BPJLT is a transistor without any PN junctions in the vertical direction. It is a gate controlled variable resistor. The characteristics of BPJLT are analyzed by varying the oxide material under the gate. It can be shown from the simulation that an ideal subthreshold slope of ~60 mV/decade can be achieved by using highk dielectric. The effects of variation of spacer length and material on the electrical characteristic of BPJLT are also investigated in the paper. The ION / IOFF ratio improvement is of the order of 107 and the OFF current reduction of 10-4 is obtained by using gate dielectric of HfO2 instead of SiO2.

**Keywords :** spacer, BPJLT, high-k, double gate
**Conference Title :** ICECECE 2014 : International Conference on Electrical, Computer, Electronics and Communication Engineering
**Conference Location :** Paris, France
**Conference Dates :** July 21-22, 2014