

Designing a Cyclic Redundancy Checker-8 for 32 Bit Input Using VHDL

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Abstract : CRC or Cyclic Redundancy Check is one of the most common, and one of the most powerful error-detecting codes implemented on modern computers. Most of the modern communication protocols use some error detection algorithms in digital networks and storage devices to detect accidental changes to raw data between transmission and reception. Cyclic Redundancy Check, or CRC, is the most popular one among these error detection codes. CRC properties are defined by the generator polynomial length and coefficients. The aim of this project is to implement an efficient FPGA based CRC-8 that accepts a 32 bit input, taking into consideration optimal chip area and high performance, using VHDL. The proposed architecture is implemented on Xilinx ISE Simulator. It is designed while keeping in mind the hardware design, complexity and cost factor.

Keywords : cyclic redundancy checker, CRC-8, 32-bit input, FPGA, VHDL, ModelSim, Xilinx

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