World Academy of Science, Engineering and Technology
International Journal of Electronics and Communication Engineering
Vol:13, No:06, 2019

A Low-Power Comparator Structure with Arbitrary Pre-Amplification Delay

Authors : Ata Khorami, Mohammad Sharifkhani

Abstract : In the dynamic comparators, the pre-amplifier amplifies the input differential voltage and when the output Vcm of the pre-amplifier becomes larger than Vth of the latch input transistors, the latch is activated and finalizes the comparison. As a result, the pre-amplification delay is fixed to a value and cannot be set at the minimum required delay, thus, significant power and delay are imposed. In this paper, a novel structure is proposed through which the pre-amplification delay can be set at any low value saving power and time. Simulations show that using the proposed structure, by setting the pre-amplification delay at the minimum required value the power and comparison delay can be reduced by 55% and 100ps respectively.

Keywords : dynamic comparator, low power comparator, analog to digital converter, pre-amplification delay
Conference Title : ICECS 2019 : International Conference on Electronic Communication Systems
Conference Location : Barcelona, Spain
Conference Dates : June 11-12, 2019