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A Floating Gate MOSFET Based Novel Programmable Current Reference

V. Suresh Babu, Haseena P. S., Varun P. Gopi, M. R. Baiju

***Abstract*-** In this paper a scheme is proposed for generating a programmable current reference which can be implemented in the CMOS technology. The current can be varied over a wide range by changing an external voltage applied to one of the control gates of FGMOS (Floating Gate MOSFET). For a range of supply voltages and temperature, CMOS current reference is found to be dependent, this dependence is compensated by subtracting two current outputs with the same dependencies on the supply voltage and temperature. The system performance is found to improve with the use of FGMOS. Mathematical analysis of the proposed circuit is done to establish supply voltage and temperature independence. Simulation and performance evaluation of the proposed current reference circuit is done using TANNER EDA Tools. The current reference shows the supply and temperature dependencies of 520 ppm/V and 312 ppm/^{o}C, respectively. The proposed current reference can operate down to 0.9 V supply.

Keywords-Floating Gate MOSFET, current reference, self bias scheme, temperature independency, supply voltage independency.

I. Introduction

PRESENT day high performance analog, digital and power electronic systems require stable, temperature independent current references. For this, many high precision, temperature compensated reference circuits have been proposed and, in particular, many efforts have been made towards developing a reliable voltage and current references in CMOS technology. For supply voltage and current independent biasing, techniques based on band gap reference is most widely used [1]-[3]. In [4], a low temperature coefficient current reference with temperature compensated resistor has been proposed. The different thermal behaviour of the threshold voltage and mobility of MOS transistors in the strong inversion region is utilized in [5] to compensate the temperature dependency. But this reference current is sensitive to supply voltage variations. In [6] two current outputs with the same supply voltage and temperature dependency are subtracted to obtain a supply and temperature compensated reference current, which shows a large temperature coefficient.

FGMOS based circuit is suitable for low voltage applications as its threshold voltage can be reduced significantly by applying voltage at one of the control gates [7], [8]. The use of floating gate transistor allows programmability of the circuit [7]-[11]. The FGMOS also provides a wide operating range and low voltage operation [10]. In this paper, we propose a FGMOS based self bias current reference circuit. The output currents from two self biased circuits having the same supply voltage and temperature dependency are subtracted to achieve the supply voltage and temperature independence. The proposed circuit shows a temperature coefficient of 312 ppm/^{0}C and supply voltage dependency of 520 ppm/V and it can work with a supply voltage as low as 0.9 V. A mathematical analysis of the proposed circuit is also presented which establishes supply voltage and temperature independence of the circuit.

The content of this paper is organized as follows. In section II, the FGMOS structure is explained. Section III describes the self biasing scheme. Section IV covers the description of the proposed current reference circuit. Section V presents the mathematical analysis of the proposed circuit. The simulation results are presented in section VI and the conclusion is made in section VII.

II. Principle Floating Gate MOSFET

FGMOS Transistor consists of a conventional MOS transistor with its gate surrounded by SiO_2 and capacitively coupled to multiple controlling input gates [12]-[15]. A two input Floating Gate MOSFET is shown in Fig. 1. A dc voltage (V_b) is applied at the Bias Gate (BG) while the signal is applied at the Signal Gate (SG). Since the gate surrounded by SiO_2 has no dc path to a fixed potential, it is known as Floating Gate, i.e. the floating gate is formed by the first polysilicon layer, while the multiple input gates are formed by the second polysilicon layer located above the floating gate. The conduction of the FGMOS transistor is different from that of conventional MOS transistor with the same terminal potential, due to the capacitive coupling between the Floating Gate (FG) and control gates. When a voltage is applied to the control gate, capacitive coupling between the control gate and FG induces an electrical field on the FG. The induced field on the FG modifies the conductance of the underlying channel region and the effective threshold voltage of the device.

The resultant threshold voltage $V_T(fg)$ of the FGMOS with respect to signal gate, depends on the threshold voltage of the

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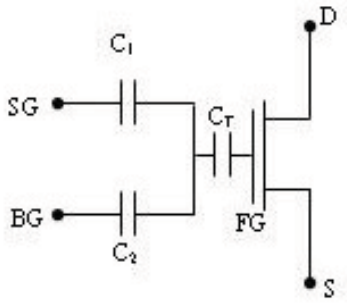

Fig 1. Two input Floating Gate MOSFET structure

Floating Gate (V_T) and is given by [9][10]

$$V_T(fg) = \frac{V_T - V_b k_1}{k_2} \quad (1)$$

where $k1 = \frac{C_1}{C_T}$, $k2 = \frac{C_2}{C_T}$, C_1 and C_2 represent the capacitances between floating gate and control gate respectively, C_T is the sum of all the capacitances between control gate and floating gate, floating gate to drain, floating gate to source and floating gate to bulk.

III. Self Bias Scheme for Current Reference

Power supply sensitivity can be greatly reduced by the use of self biasing. The block diagram in Fig. 2 illustrates the concept of self bias [16]. In this scheme, instead of developing the input current by connecting a resistor to the supply, the input current is made dependent directly on the output current of the current source itself. Assuming the feedback loop formed by this connection has a stable operating point, all the current flowing in the circuit is much less sensitive to power-supply voltage than that of the resistively biased case.

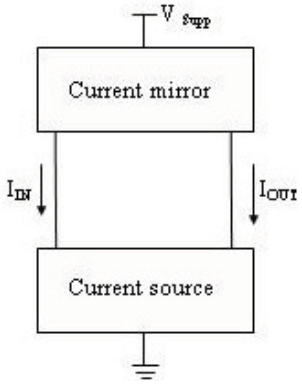

Fig 2. Self bias scheme for current reference

IV. The Proposed Current Reference Circuit

The proposed current reference circuit based on FGMOS is depicted in Fig.3. The circuit consists of two self biased current reference circuits and one current subtraction circuit. The first self bias circuit is made up of the current mirror M_3-M_4 and the current source $M_1-M_2-M_5-R_1$. The temperature drift due to R_1 is compensated by placing M_5, with a voltage drop equal to sum of two terms having opposite temperature coefficients. The current mirror fixes the ratio m_1 (current ratio between M_3 and M_4) between the current flowing in the two branches and the current source defines the value of current I_1. Similarly the second self bias current reference consists of the current mirror M_8-M_9 which fixes the ratio m_2 (current ratio between M_8 and M_9) and the current source $M_6-M_7-M_{10}-R_1$ which defines the current I_2. The temperature drift due to R_1 in this circuit is compensated by M_{10}. The two self biased current references generate I_1 and I_2 respectively. The current mirror M_4 and M_{11} multiplies I_1, to get NI_1 and the current mirror M_9 and M_{12} multiplies I_2 to get MI_2. Then, by subtracting MI_2 from NI_1, the supply and temperature compensated output current is obtained.

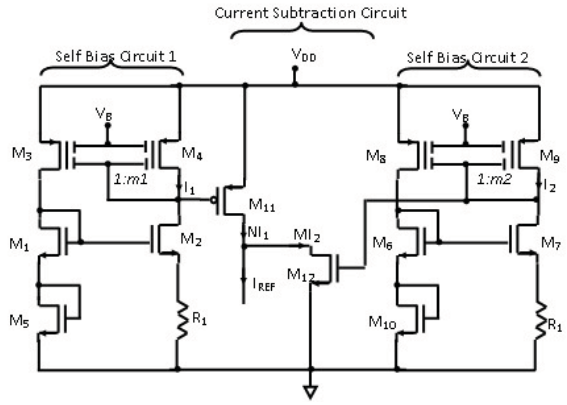

Fig 3. The proposed current reference circuit

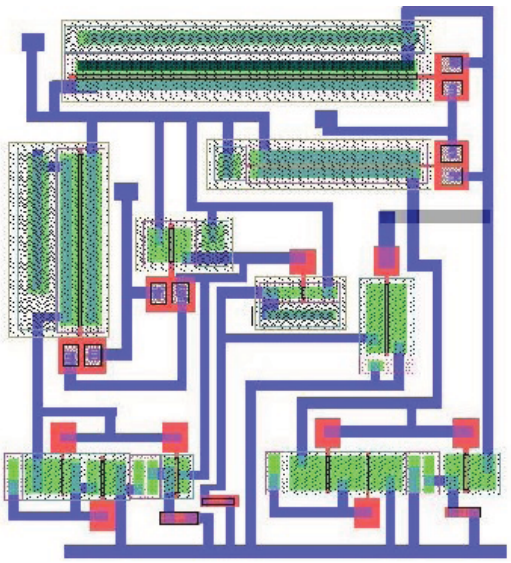

Fig 4. Layout of the proposed current reference circuit

V. Mathematical Analysis

MOS transistors in the proposed circuit works in saturation region. Therefore the drain current I can be expressed in terms of their gate to source voltage as

$$I = \frac{\mu C_{ox}}{2}\frac{W}{L}(V_{GS} - V_T)^2 \tag{2}$$

where μ is the mobility of electrons (holes) in NMOS (PMOS) devices, C_{ox} is the gate capacitance per unit area, W/L is the aspect ratio of the MOS device with W as the gate width and L as the gate length, and V_T is the threshold voltage. From (2) V_{GS} is obtained as

$$V_{GS} = V_T + \sqrt{\frac{I}{\beta_0 \alpha}} \tag{3}$$

where $\beta_0 = \frac{\mu C_{ox}}{2}$ and $\alpha = \frac{W}{L}$ Applying Kirchoff's voltage law to the current source in the first self biased circuit leads to

$$V_{GS1} + V_{GS5} - V_{GS2} - m_1 R_1 I_1 = 0 \tag{4}$$

Substituting the value of V_{GS} in (4) results in (5)

$$\sqrt{\frac{I_1}{\beta_0}}\left(\frac{1}{\sqrt{\alpha_1}} + \frac{1}{\sqrt{\alpha_5}} - \sqrt{\frac{m_1}{\alpha_2}}\right) + V_T - m_1 R_1 I_1 = 0 \tag{5}$$

Here the voltage drop across resistor R_1 is given by the sum of two terms with different temperature coefficients. One term is related to the overdrive voltage of the transistors M_1, M_2 and M_5 and has a positive temperature coefficient due to the negative temperature drift of mobility, while the other term is the threshold voltage V_T which has a negative temperature coefficient. Therefore, by properly choosing R_1 a temperature compensated current I_1 is obtained.

Squaring (5),

$$m_1^2 R_1^2 I_1^2 - 2m_1 R_1 I_1 V_T + V_T^2 = \frac{I_1}{\beta_0}\left(\frac{1}{\sqrt{\alpha_1}} + \frac{1}{\sqrt{\alpha_5}} - \sqrt{\frac{m_1}{\alpha_2}}\right)^2 \tag{6}$$

Equation (6) is a quadratic equation in I_1. Neglecting higher powers of R_1 result in an approximated solution, given by

$$I_1 = \frac{V_T}{m_1 R_1} + \frac{1}{2\beta_0 m_1^2 R_1^2}\left(\frac{1}{\sqrt{\alpha_1}} + \frac{1}{\sqrt{\alpha_5}} - \sqrt{\frac{m_1}{\alpha_2}}\right)^2 \tag{7}$$

Setting $\alpha_1 = \alpha_2 = \alpha_5 = \alpha$ in (7),

$$I_1 = \frac{V_T}{m_1 R_1} + \frac{1}{\beta R_1^2}\left(\frac{1}{m_1} - \frac{1}{2\sqrt{m_1}}\right)^2 \tag{8}$$

where $\beta = \beta_0 \alpha$.

Similarly for the second self bias current reference circuit the current I_2 is given by

$$I_2 = \frac{V_T}{m_2 R_1} + \frac{1}{2\beta_0 m_2^2 R_1^2}\left(\frac{1}{\sqrt{\alpha_6}} + \frac{1}{\sqrt{\alpha_{10}}} - \sqrt{\frac{m_2}{\alpha_7}}\right)^2 \tag{9}$$

In (9), setting $\alpha_6 = \alpha_7 = \alpha_{10} = \alpha$,

$$I_2 = \frac{V_T}{m_2 R_1} + \frac{1}{\beta R_1^2}\left(\frac{1}{m_2} - \frac{1}{2\sqrt{m_2}}\right)^2 \tag{10}$$

The reference current is obtained by subtracting the current MI_2 from NI_1 as in (11)

$$I_{ref} = NI_1 - MI_2 \tag{11}$$

Substitution of (8) and (10) in (11) results in (12)

$$I_{ref} = \frac{V_T}{R_1}\left(\frac{1}{m_1} - \frac{1}{m_2}\right) + \frac{1}{\beta R_1^2}\left[N\left(\frac{1}{m_1} - \frac{1}{2\sqrt{m_1}}\right)^2 - M\left(\frac{1}{m_2} - \frac{1}{2\sqrt{m_2}}\right)^2\right] \tag{12}$$

In (12) as expected, the reference current is independent of supply voltage. Also, due to the negative coefficient of first term and positive temperature coefficient of the second term, temperature dependency is reduced.

VI. Simulation Results and Discussion

The layout of the proposed circuit is shown in Fig. 4. The layout is prepared by using LEDIT tool provided by TANNER EDA. The simulation of the proposed current reference circuit is carried out using TSPICE in TANNER EDA with BSIM 4.4 model card. Fig. 5 shows the variation of reference current, I_{ref}, NI_1 and MI_2 with supply voltage. From this figure we can see that I_{ref} which is the difference between NI_1 and MI_2 is constant over a range of supply voltages. Fig. 6 shows the variation of I_{ref}, NI_1 and MI_2 with temperature. Here also, I_{ref} is found to be constant over a range of temperature. From these results, temperature coefficient and supply voltage dependence are calculated as 312 ppm/^{o}C and 520 ppm/V respectively. The performance of the proposed current reference circuit is compared with the current reference circuits in [5] and [6] for output current, supply voltage requirement, temperature dependency. The comparison is tabulated in Table I.

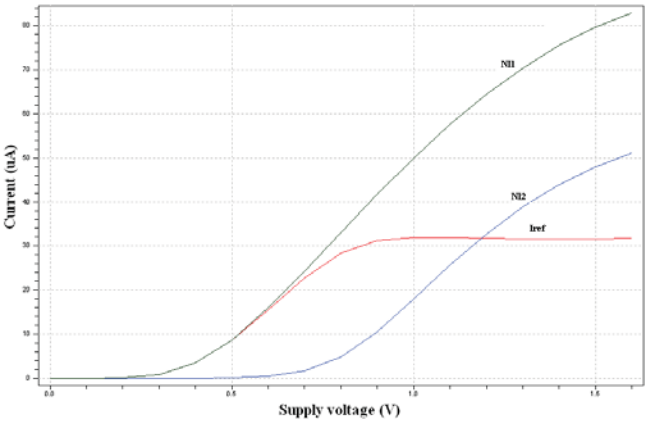

Fig 5. Variation of Reference current I_{ref}, NI_1 and MI_2 with Supply Voltage

The data in Table I shows that, the proposed circuit has better performance compared to the previous works in terms of supply voltage requirement, supply voltage and temperature dependence of current output.

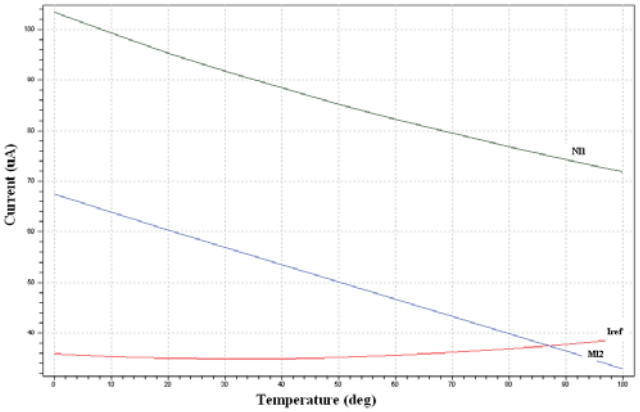

Fig 6. Variation of Reference current I_{ref}, NI_1 and MI_2 with Temperature

TABLE I
PERFORMANCE COMPARISON OF CURRENT REFERENCE

Parameter	Unit	Proposed	[5]	[6]
Output current	μA	31.8	13.65	10.45
Minimum supply voltage	V	0.9	2.5	1.1
Supply dependency	ppm/V	520	4000	1700
Temperature dependency	ppm/^{0}C	312	130	720
Temperature Range	^{0}C	0-100	-30-100	0-120

VII. Conclusion

A novel FGMOS based current reference is proposed in this paper. The dependence of current reference on supply voltage and temperature is compensated by subtracting two current outputs having same dependencies on supply voltage and temperature. Mathematical analysis also establishes the same. The layout of the proposed current reference circuit is prepared using LEDIT tool provided by TANNER EDA. TSPICE simulation results using BSIM 4.4 model card are presented. Simulation result shows that the reference current has a temperature dependency of 312 ppm/^{0}C in the temperature range 0-100^{0}C and a supply dependency of 520 ppm/V. The circuit is found to be operating at a supply voltage as low as 0.9 V.

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