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Transient Enhanced LDO Voltage Regulator with Improved Feed Forward Path Compensation

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***Abstract*—**Anultra-low power capacitor less low-dropout voltage regulator with improved transient response using gain enhanced feed forward path compensation is presented in this paper. It is based on a cascade of a voltage amplifier and a transconductor stage in the feed forward path with regular error amplifier to form a composite gain-enhanced feed forward stage. It broadens the gain bandwidth and thus improves the transient response without substantial increase in power consumption. The proposed LDO, designed for a maximum output current of 100 mA in UMC 180 nm, requires a quiescent current of 69 µA. An undershot of 153.79mV for a load current changes from 0mA to 100mA and an overshoot of 196.24mV for current change of 100mA to 0mA. The settling time is approximately 1.1 µs for the output voltage undershooting case. The load regulation is of 2.77 µV/mA at load current of 100mA. Reference voltage is generated by using an accurate band gap reference circuit of 0.8V.The costly features of SOC such as total chip area and power consumption is drastically reduced by the use of only a total compensation capacitance of 6pF while consuming power consumption of 0.096 mW.

***Keywords*—**Capacitor-less LDO, frequency compensation, Transient response, latch, self-biased differential amplifier.

I. Introduction

THE market demand for portable consumer electronics products like laptops, smart phones, video cameras, tablets is exponentially growing. The different blocks of these products demand for increased processing power for a longer period of time and switching functionality response to signal variations [1].Power Management being an essential requirement, and as part of solution, is rapidly changing in order to meet these rigorous demands. Low drop out voltage regulators (LDOs) being essential part of power management unit meet the demands by reducing the quiescent current consumption and footprint area of the chip [2].

Although, conventional voltage regulators has the advantage of lower voltage operation and higher power efficiency but its larger output capacitor of microfarad range creates a low frequency pole which acts as dominant pole and slows down the dynamic response behavior [3], [4]. Capacitor less LDO constituting internal capacitor of range of ten to hundreds of picofarad being the alternative aims to circumvent the non-desirable characteristics of conventional LDO and achieves the best performance in terms of power consumption and chip area. However, the stability of system is degraded as pole set by smaller capacitor is no longer the dominant one. The dominant pole depends on the topology set by the error amplifier or buffer connected to the pass device gate. The shift of dominant pole and zero back to location below unity gain frequency (UGF) and non-dominant poles put forth beyond UGF attains the stability of system. Thus, a frequency compensation scheme maintaining system for the full range of load current is in great need. Much research has been conducted on different compensation topologies and techniques for LDO stabilization without the large external capacitor. All of the presented strategies rely on detecting the output current or voltage and applying suitably to the gate of pass transistor for performance improvement.

Nested miller compensation topologies employing compensation capacitors in the feedback loop for the three stages amplifier attains desired phase margin and transient response but trade-offs between bandwidth and slew rate takes place [5]. They employed 500pFcapacitor at the output node for stability purpose but not suitable for low power environment. Surkanti's and Kwok's studies[6], [7]revealed that by cancelling the effect of existent out pole by determining its location and dynamically adding a zero over it using Resistor–Capacitor (RC) series connected to the gate of the pass device. This achieves greater bandwidth for a suitable phase margin and also improves slew rate. However, complexity, quiescent current and silicon area are significantly higher.

The technique reported by Leung [8], [9] relies on pole splitting compensation technique that assures that the zero of the system is well below the UGF and high frequency poles are at least three times larger than UGF. The concept utilized is to use the transconductance of pass device and low output node capacitance for achieving stability but the achieving of large transconductance of pass transistor in drop out condition is extremely difficult to be achieved and involved extra stages which increases the complexity. However, this topology achieves higher bandwidths than the other techniques presented for a given low quiescent current.

The topology represented by Ming [10] concept involves injecting more transient current in the biasing circuitry adaptively. As, the biasing current is controlled by the capacitive coupling path precise adjustment is required for proper operation. The adaptive biasing will provide higherbandwidth and a larger slew rate. But, the fast transient current injected in the bias circuitry will increase the quiescent current of the LDO demanding more compensation at times and added complexity.

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In feed forward-based LDO , maintaining high bandwidth for faster transient response needs substantial increase of feed forward transconductance for counteracting the right-hand plane (RHP) zero, and hence, higher power consumption. The reported topologies may not be suitable for tradeoff between gain bandwidth and power dissipation at the same time. Based on these observations, this raises the motivation in devising an improved compensation methodology to meet the challenges for low-power bandwidth efficiency as well as small silicon area.

To achieve the objectives, apart from a class AB error amplifier employed for improved performance in the basic feedback loop, a feed forward path constituting wideband gain enhanced voltage amplifier with low impedance in series with a transconductance stage is used. Hence, the overall feed forward transconductance is enhanced by a gain factor of Av. The resultant of which improves the amplifier performance on maximizing bandwidth at the low power constraint together with only small compensation capacitance, to keep the amplifier stable. The proposed technique and its analysis are described in Section II. Section III details the implementation of the structure. This is then followed by results, and performance comparisons in Section IV. Finally, the concluding remarks are given in Section V.

II. Proposed LDO Topology

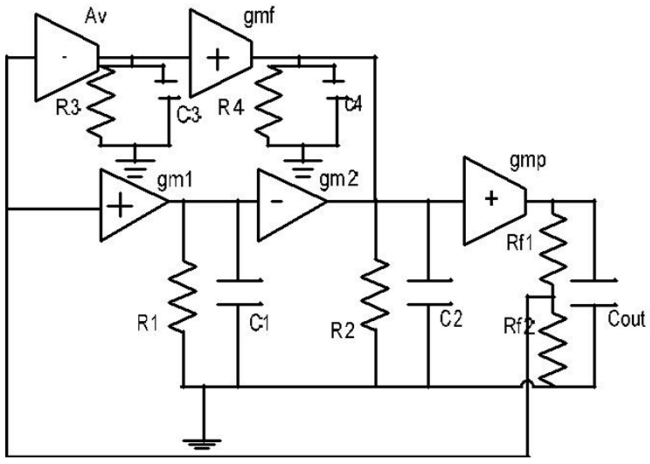

Fig. 1 Block diagram of the proposed LDO voltage regulator

The proposed block diagram of the closed loop LDO voltage Regulator with gain enhanced feed forward path compensation is shown in Fig. 1. It consists of two stage error amplifier of class AB structure with enhanced slew rate features embedded. The gm1, gm2, gmf represent the transconductance of the stages. The output equivalent resistances and equivalent capacitances are R1, R2, R3, R4 and C1, C2, C3 and C4 respectively. The pass transistor transconductance is gmp and output resistances are Rf1and Rf2.The basic loop along with fast reacting loop act together to enhance the transient response of LDO.

III. Proposed Transistor Level Implementation

The transistor level implementation of the proposed LDO is shown in Fig. 2.The error amplifier constitute transistors M0-M6,M21,M22 and capacitors c1,c2,c3 while M7-M24 constitute high gain broadband width amplifier and transconductancegmf.The pass transistor is represented by Mp while feedback resistances by Rf1 and Rf2.

The slew rate of error amplifier is primarily limited by the input stage current and the compensation capacitors usage for maintaining stability. Further, the conventional error amplifiers employed in state of art LDOs operate as class A amplifiers which limit their slew rate. The capacitor less LDOs requiring high slew rate at the gate of pass transistor for good transient response, need to have amplifiers operating in class AB.The proposed circuit modification provides means for achieving this by employing low value of total compensation capacitance and less power consumption.

As the load current changes from 0 to 100 mA, output voltage experiences undershoot. The sampled voltage is feedback back to the input gate of transistor M1.Due to differential action a current nearly equal to 2I flows to the gate of pass transistor through two paths.First, it flows through C1 whose value is chosen deliberately to be much larger than C2. This drives the gate capacitance of pass transistor forcing M5 to be relatively cutoff due to transient voltage. Then, for a short interval, the, charge stored in the gate capacitance of pass transistor raises the source potential of transistor M22 but not sufficiently high to turn it on. As a result, the slew rate at the gate of pass transistor is moderate enough. Second, M6 current has risen in the meantime due to the capacitor c2 acting as low impedance for the large transients; so the slewing is little faster. As the threshold of transistor M22 is passed slew rate gets limited by the total miller capacitance across M6 rather than the gate capacitance of pass transistor. The M22 transistor acting as switch shorted the gate of M5 and M6 and the total transconductance at the output stage of error amplifier is increased (gm5+gm6).It is to be noted that M22 will go into conduction before M3 enters triode region mode; therefore, the 2I current drive will be substantially maintained by M3 for operation [11].

The feed forward path of error amplifier and pass transistor does improve the slew rate at the gate of pass transistor for transients of low magnitude undershoot. But for large transients, the second feed forward path constituting gain enhanced voltage amplifier driving a transconductor is utilized to drive the gate of pass transistor which acts a fast reacting path to substantially reduce the transients.

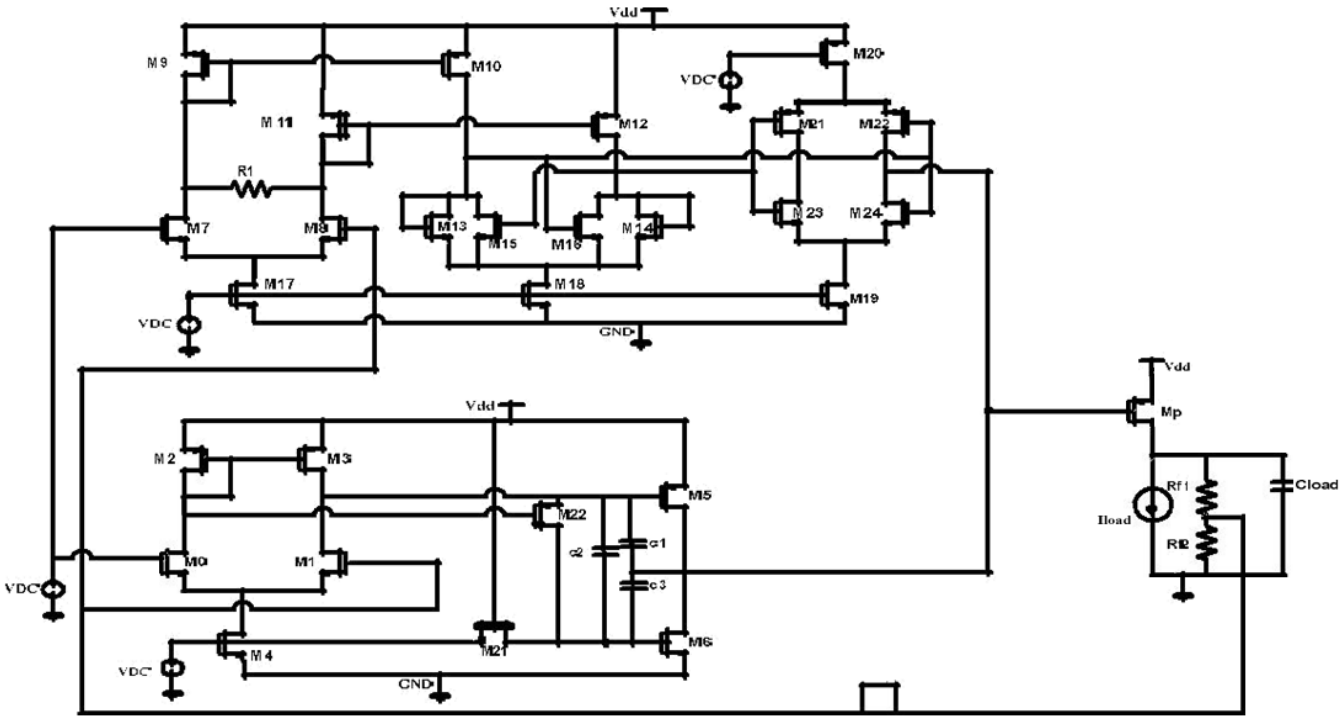

Fig. 2 Schematic of the proposed LDO voltage regulator

In order to achieve bandwidth and area efficient amplification, the voltage-gain stage should have the attributes of low power, broad bandwidth and high gain as well as small silicon area. This is achieved by using transistors M17-M18 transistors as broadband width amplifier. If the input to the amplifier from feedback is slightly larger than Vref, then the function of further stages is to amplify the input with as little per stage as possible. The role of transistors M9 and M11 is to build up the initial change to a sufficient large value and then apply it to latch which further enhances the gain to significant value in a short span of time.

But, the output of latch should drive a large value of capacitance at the gate of pass transistor which is not sufficient. In this case, it is advisable to follow the latch by circuits that can quickly generate large amounts of current [12].

A conventional CMOS differential amplifier cannot provide switching currents that exceed the quiescent current set by the current-source device set by the M20 which operates in saturation region. The capability of supplying momentarily large current pulses makes this M19-M24 especially suitable for rapidly charging and discharging the gate capacitance without at the same time consuming inordinate amounts of power [13].

IV. Simulation Results

The proposed LDO voltage regulator has been simulated with 0.18µm CMOS technology. The compensation capacitor c1, c2, c3 is of small value of 1, 4, 3pF respectively. The feedback resistors Rfb1, Rfb2 are 30 kΩ and 60 kΩ respectively. The output voltage is 1.4V while the reference voltage is 800 mV generated using band gap reference circuit.

A. Transient Response

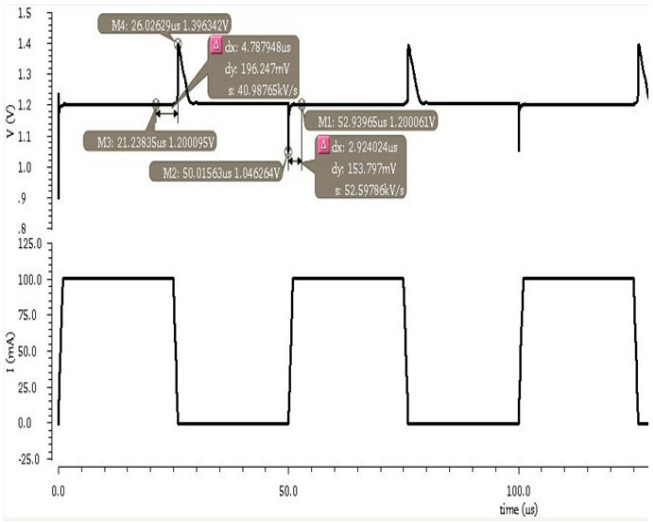

Fig. 3 Load current transient

The simulation was performed at the minimum dropout voltage where the output current quickly (rise/fall time=1 µs) varied from 0 mA to 100 mA.

An undershot of 153.79mV and 196.24mV can be observed for the load current change of 0 to 100mA.

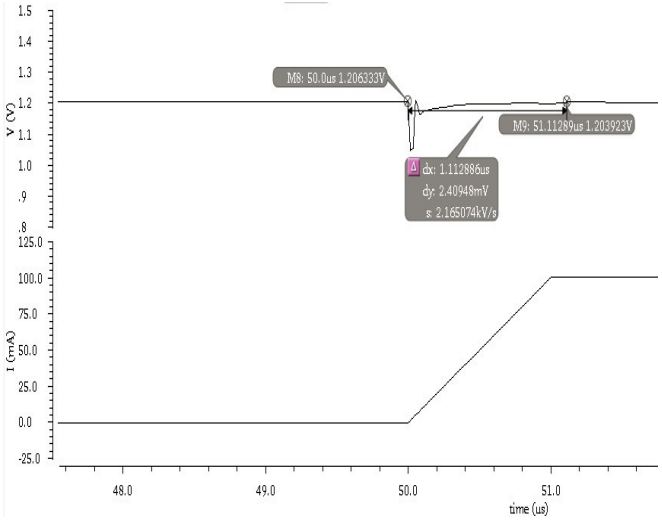

Fig. 4Settlingtime of transient response

The settling time, as shown in Fig. 4, is approximately 1.1 µs for the output voltage undershoot case.

B. Frequency Response and Phase Margin

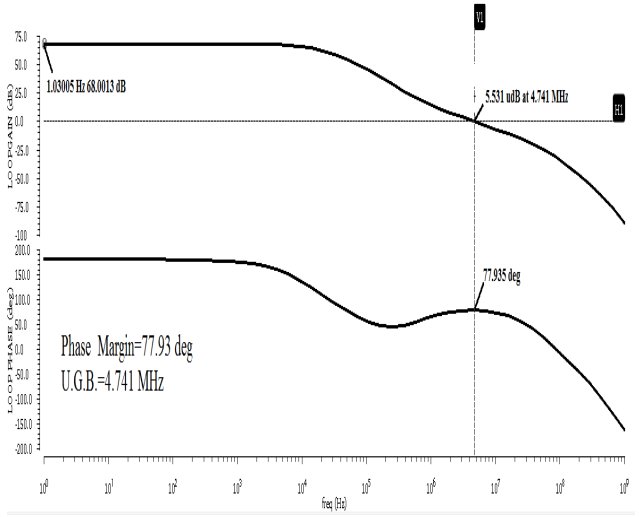

Fig. 5 Gain and phase response

The frequency response of the proposed LDO is presented in Fig. 5. With the load current 100mA, the UGF is 4.742 MHz; the loop gain is around 68.0dB, and phase margin of 77.93°. Simulation results exhibit the existence of single dominant pole within UGF. The minimum phase margin is always larger than 50° for the entire load current range, thus, the stability of the closed loop is ensured.

C. Transient Response

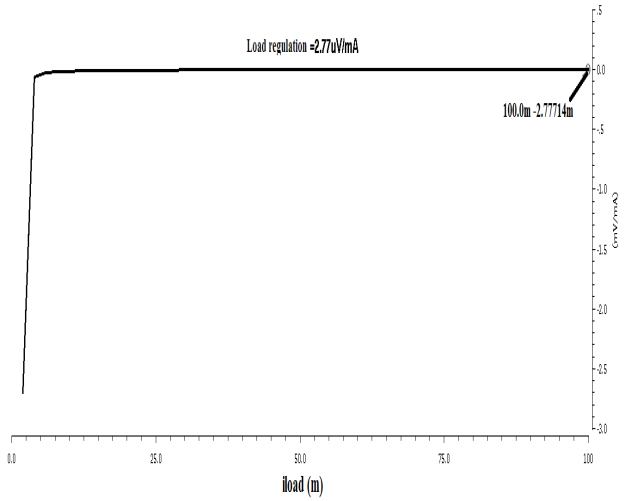

Fig. 6 Load Regulation

The output voltage is around 1.8V when the load current varies from 0 to 100 mA, with load regulation of 2.77 µV/mA at 100mA load current.

TABLE I
COMPARISON OF THE CAPACITOR-LESS LDO TOPOLOGY AGAINST THE STATE OF ART

Reference	[14]	[15]	[16]	[17]	[18]	[This work]
Year	2009	2011	2012	2013	2014	2014
Tech.(µm)	0.35	0.18	0.35	0.11	0.18	0.18
Voltage drop (mV)	200	200	150	200	200	200
Cout (pF)	100	0-100	100	40	100	100
Load Regulation (µV/mA)	1.8	19.54	80	108	70	2.77
Imax (mA)	100	100	100	200	100	100
Imin (µA)	50	0	0	500	0	0
IQ (µA)	27-270	14-53.5	7	41.5	3.7	69
ΔVout (mV)	500	<399	236	385	277	153.79
Settling time (µs)	0.3	3.96	0.15	77	6	1.11

V. CONCLUSION

LDO voltage regulator with a gain enhanced feed forward stage to broaden the loop gain bandwidth without increasing power consumption is introduced. With the proposed technique, the transient response is drastically improved and exhibits an undershoot of 153.79mV and overshoot of 196.24mv with a total quiescent current of 65µA.The output load transient is recovered within 1.1µs.Besides,simulation results have shown good stability with a phase margin of 77.93°, with absence of peaking effect. The improved design will be suitable for SoC applications to reduce power and cost consumption.

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