World Academy of Science, Engineering and Technology
International Journal of Electronics and Communication Engineering
Vol:8, No:9, 2014

Application of Hardware Efficient CIC Compensation Filter in Narrow Band Filtering

Vishal Awasthi, Krishna Raj

***Abstract*—**In many communication and signal processing systems, it is highly desirable to implement an efficient narrow-band filter that decimate or interpolate the incoming signals. This paper presents hardware efficient compensated CIC filter over a narrow band frequency that increases the speed of down sampling by using multiplierless decimation filters with polyphase FIR filter structure. The proposed work analyzed the performance of compensated CIC filter on the bases of the improvement of frequency response with reduced hardware complexity in terms of no. of adders and multipliers and produces the filtered results without any alterations. CIC compensator filter demonstrated that by using compensation with CIC filter improve the frequency response in passed of interest 26.57% with the reduction in hardware complexity 12.25% multiplications per input sample (MPIS) and 23.4% additions per input sample (APIS) w.r.t. FIR filter respectively.

***Keywords*—**Multirate filtering, Narrow-band Signaling, Compensation Theory, CIC filter, Decimation, Compensation filter.

I. Introduction

MULTIRATE signal processing techniques are used in numerous applications such as video compression, digital audio, multimedia, speech processing and wireless communication etc. The field of DSP has always been driven by scaled-VLSI technologies. Different algorithms are used in various real-time applications with different sampling rate that can vary from 20 KHz in speech processing to over 500 MHz in radar applications. FIR filter is one of the fundamental processing elements in any signal processing system. In some application such as video processing, the filter circuit must be able to operate at high frequencies, while in other application, such as cellular telephony, the circuit must be a low-power with high throughput. Normally the frequency band of over 1GHz is used for fixed high-speed data communication such as Wireless LAN, while the frequency band less than 1GHz is well suited for low or medium-speed mobile communication.

Fast sampling rate offers several benefits, including the ability to digitize wideband signals, reduced complexity of anti-alias filters, and lower noise power spectral density. The decimation filter (decimator) is a sampling rate conversion system, performs low-pass filtering as well as down-sampling operation and hence widely used in speech processing and communication systems application. Now in the last few years considerable attention has been focused on the design of high efficiency decimation filters in different applications.

Hogenauer [1] presented a commonly used decimation filter known as cascaded-integrator-comb (CIC) filter that consists of cascaded integrators and differentiators section, separated by a down-sampler. This multiplierless filter has very low complexity, but exhibits two main problems: (a) The Integrator section works at the higher input data rate while the differentiator section operates at the lower data rate and therefore require a higher chip area with higher power dissipation and (b) A high passband droop and low stopband attenuation in its magnitude characteristic. A pictorial representation of the decimation process is shown in Fig. 1:

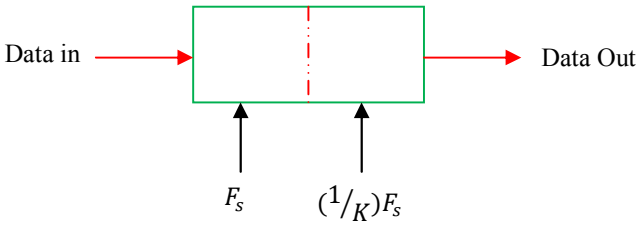


Fig. 1 Conceptual view of a decimation filter

For decimation by a factor of K, the original data must reside in a bandwidth given by $F_s/(2K)$, where F_s is the rate at which the original data was sampled. Thus, if the original data contains valid information in the portion of the spectrum beyond $F_s/(2K)$, decimation is not possible. The three basic tasks performed by decimation filter are: (a) Removing quantization noise (b) Decimation (sample rate reduction) (c) Anti-aliasing.

Higher order modulators produce highly shaped noise and hence the decimation filter should be very efficient to remove this excess quantization noise and to regain the original characteristics of the signal in the base band.

To overcome these problems, various methods have been introduced that uses the non - recursive structure of a comb filter to reduce the power consumption as well as to increase the circuit speed. Johansson, H. et al. discussed the previously proposed low pass narrow-band, wideband filters and masking FIR filters and propose a design method for high pass narrow-band filters. The proposed approach uses a single hardware structure using folding algorithm to give an area-efficient implementation with a small number of multipliers and adders at the cost of more memory [2]. Kwentus et al. [3] outlined a method that uses the sharpening technique to decrease the passband droop and to increase the stopband attenuation, but it

Vishal Awasthi is with the Electronics and Communication Engineering Department, UIET, C.S.J.M. University, Kanpur-24 (U.P.), India (corresponding author e-mail: awasthiv@rediffmail.com).
Krishna Raj is with the Electronics Engineering Department, H.B.T.I., Kanpur (U.P.), India (e-mail: kraj_biet@yahoo.com).

requires sharpening to be performed at the high input rate and hence resulting higher power consumption.

An implementation of narrowband lowpass FIR filter with a significantly reduced number of multiplications per second with less round off noise and less severe coefficient sensitivity problems than a standard FIR filter implementation is described in [4], [5].

Jovanovic et al. [6] discussed some methods to attain the desired low stopband attenuation by allowing the sharpening section to operate at the lower rate with the cost of the introduction of two multipliers working at a high rate. Kayano, H. et al. proposed a transmitting hybrid narrow-band filter consists of superconducting resonators and conventional cavity for of Radar application [7]. A very efficient recursive structures to implement the Classes of linear-phase finite-impulse response (FIR) filters with a piecewise-polynomial impulse response is proposed in [8], [9]. The arithmetic complexity of these filters is proportional to the number of branches and the common polynomial order for each branch, rather than the actual filter order. The proposed filter reduced number of multipliers in optimized manner in the actual implementation. Neuvo, Y. et al. derived a computationally efficient realization of a symmetrical bandpass FIR filter, composed of two cascaded FIR sections. In [10] a new multistage comb-rotated sinc (RS) decimator is introduced which permit both multipliers to work at the lower rate, with no filtering at the high input rate. In [11], G. Javanovic Dolecek et al. proposed an efficient modification of the CIC cosine decimation filter using canonical signed digits (CSD). In narrow-band implementations, the number of multipliers and adders is approximately inversely proportional to the desired relative transition bandwidth. The structure allows simple tuning of the center frequency of the band pass filter and has good finite wordlength properties [12].

In this paper, the hardware complexity of the CIC compensator filter with FIR filter is analyzed on the bases of the no. of adders and multiplier used in a block to improve the frequency response in passed of interest for fast down sampling.

The organization of the paper is as follows. In Section II we define the efficient structure of Cascaded Integrator Comb (CIC) filter with some basic needs of Narrow band communication. Sections III & IV describe the CIC Compensation filter with different compensation techniques. The design issue and performance analysis are provided in Section V. The result analysis of different decimation filter structures is discussed in section VI. The discussion and conclusion of the paper are described in Section VII.

II. Cascaded Integrator Comb (CIC) Filter

Narrow band communication is widely applied to realize stable long-range communication with the high carrier purity of transmission spectrum and therefore it leads the high efficiency of radio wave use within the same frequency band. Narrow band communication is the optimal in the site where many radio-control equipments are used, but this communication is limited in some aspects such as:

(a) Since the receiver bandwidth is narrow, it is difficult for high-speed data communication.
(b) Generally, data speed is limited less than 9600 bps, and the request for frequency stability is several PPMs.
(c) As a frequency standard, temperature compensation is necessary for the crystal oscillation circuit.
(d) The cost and size of Narrow band Radio module are higher than wideband one-chip radio IC as it is constituted of discrete components.

Modern base station transceivers perform channel access using a digital down-converter (DDC) to support multicarrier environments or for coherently down converting and combining a number of narrow-band channels into one wideband digital signal. The baseband channel is highly oversampled, so a simple cascade of boxcar filters, implemented as a cascaded integrator comb (CIC) filter, proposed by Eugene Hogenauer [1], will be employed to initially reduce the sample rate.

The cascaded integrator-comb (CIC) filter is a class of hardware-efficient linear phase finite impulse response (FIR) digital filters in terms of multipliers and adders. CIC filters have the property to get sampling rate decrease (decimation) and sampling rate increase (interpolation) without employing any multipliers. Its frequency response is tunable as selecting the appropriate number of cascaded integrator and comb filter pairs. As the CIC filter doesn't have a flat pass band response, this disadvantage is removed by using compensation filter. However, the disadvantage of a CIC filter is that its pass band is not flat, which is undesirable in many applications. Fortunately, this problem can be alleviated by a compensation filter. The CIC filter first performs the averaging operation, then follows it with the decimation. The transfer function of the CIC filter in z-domain is given in (1):

$$H[z] = H[z]_I^p . H[z]_C^p = \frac{(1-z^{-K})^p}{(1-z^{-1})^p} = \left(\frac{1-z^{-K}}{1-z^{-1}}\right)^p \quad (1)$$

In (1), K is the oversampling ratio and p is the order of the filter. The numerator $(1-z^{-K})^p$ represents the transfer function of a differentiator and the denominator $1/(1-z^{-1})^p$ indicates the transfer function of an integrator.

A simple block diagram of a first order CIC filter is shown in Fig. 2. In a CIC filter, the integrators operate at a high sampling frequency (f_s), and the comb filters operate at low frequency $(\frac{f_s}{K})$. The clock divider circuit divides the oversampling clock signal by the oversampling ratio, K after the Integrator stage. By operating the differentiator at lower frequencies, a reduction in the power consumption is achieved.

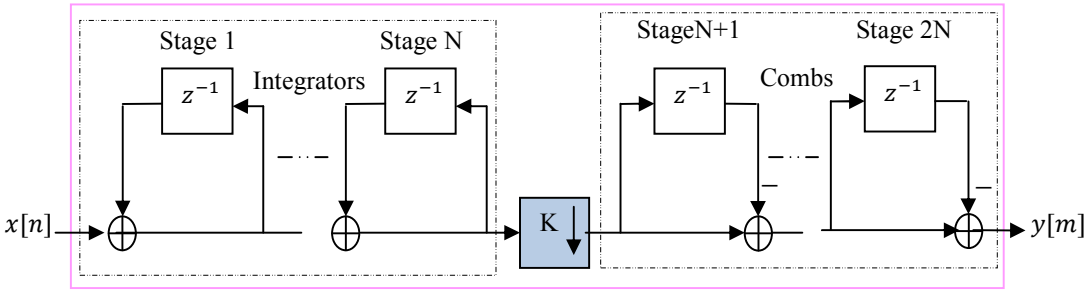


Fig. 2 Block diagram of first order CIC filter

III. CIC Compensation Filter

To ensure high system clock frequencies, the CIC decimator is actually implemented using the pipelined architecture in which there is only a single adder between registered nodes. This can potentially lead to operating speed issues in some technologies because of the serial dependency in the adder / subtractor carry chains. Modern FPGA devices like Virtex-II provides extremely high performance carry chains and even the long carry-chains that can be required in some CIC filters can be supported at very high speed.

Increased number of stages does not lead to wide and flat pass band frequency response of CIC filters. To overcome the resulting response, an FIR filter that has a magnitude response that is the inverse of the CIC filter can be applied. Such filters are called "compensation filters." For down sampling, the compensation filter follows the CIC filter and for up sampling systems, the compensation FIR filter is placed before a CIC filter. In other words, the compensation filter always operates at the lower rate in a rate conversion [4], [13].

IV. Different Compensation Techniques

When the number of stages is large, CIC filter introduces a droop in the passband and this droop is dependent on the CIC decimation ratio. To overcome the magnitude droop, an FIR filter that has a magnitude response that is the inverse of the CIC filter can be applied to achieve frequency response correction. Usually the CIC filter is followed by a second decimating lowpass filter stage and its decimation ratio is significantly smaller than that of the CIC stage (typically 16 or less). The decimation factor of this second stage will determine the frequency at which the worst-case aliasing will occur and will also determine the edge frequency of the passband of interest, where the worst-case passband distortion will occur. Several schemes have been proposed to design the compensation of CIC filter's passband droop, mainly in the narrow pass band. The motivation behind the compensation methods is to appropriately modify the original CIC characteristic in the pass band such that the compensator filter has as low complexity as possible. The various methods used for compensation of CIC decimation filter [14] are as follows:

A. CIC Roll-Off Compensation filter

The CIC roll- off compensation filter [16] is like a channel selective filter with symmetric characteristics in frequency response. This method compensated the roll off of the CIC filter in pass band by letting the CIC filter followed by a symmetric FIR filter with a minimum order. CIC roll off compensation filter can be written as:

$$c(n) = \frac{-v}{1-2v}\delta(n+1) + \frac{1}{1-2v}\delta(n) + \frac{-v}{1-2v}\delta(n+1) \quad (2)$$

where $\left[\frac{-v}{1-2v}, \frac{1}{1-2v}, \frac{-v}{1-2v}\right]$ are the compensation filter coefficients and $C(w) = \frac{1-2vcosw}{1-2v}$ is its frequency response.

The performance of the compensation filter depends on the value of v, which is obtained by minimizing the corresponding error function. $C(w)$ can work as a roll off compensation filter as it shows opposite frequency characteristics of the CIC filter in the frequency domain. Let the frequency response of the CIC filter as $f(w)$, P_e is pass band edge of the received signal and the frequency response of an ideal filter as D(ω), then error function is defined by-

$$E_{uw(v)} = \int_0^{P_e} (D(w) - C(w)f(w))^2 dw \quad (3)$$

Roll off phenomenon of the CIC filter can exactly compensated if the frequency response characteristics of the received signal are used as a weighting function. It slightly improves the flatness of the pass band. This method focused on compensating the slope of the pass band, which is already fixed in the digital receiver, by letting the CIC filter followed by the compensation filter with a minimum computational load.

B. Compensated CIC-Cosine decimation filter

This filter is a modified and efficient version of the CIC Cosine decimation filter [11], [17]. In order to improve the passband of interest of the overall filter, a second order compensator filter is introduced at low rate. The compensator filter coefficients are presented in a canonical signed digit (CSD) form, and can be implemented using only adders and shifts. Transfer function and magnitude response of compensation filter are given by-

$$H_{comp}(z^M) = v + uz^{-M} + vz^{-2K} \quad (4)$$

$$\left|H_{comp}(e^{jKw})\right| = |2v\cos(Kw) + u| \quad (5)$$

where v & u real valued constant and K are is decimation factor. Worst pass band distortion occurs at $w = 0$ & $w = w_c$

where $w_c = \frac{\pi}{KR}$ and R is the decimation factor of the next decimation stage. In order to compensate the pass band droop (δ_c) at the frequency w_c then $2v + u = 1$ and $2\cos(Kw_c) + u = \frac{1}{\delta_c}$. v *and* u can be calculated-

$$\begin{bmatrix} v \\ u \end{bmatrix} = \begin{bmatrix} \frac{-1}{2(\cos(Kw_c)-1} & \frac{1}{2(\cos(Kw_c)-1} \\ \frac{\cos(Kw_c)}{(\cos(Kw_c)-1} & \frac{-1}{(\cos(Kw_c)-1} \end{bmatrix} \begin{bmatrix} 1 \\ \delta_{comp} \end{bmatrix} \quad (6)$$

$$v = \frac{-1+\delta_{comp}}{2(\cos(Kw_c)-1} \quad (7)$$

$$u = \frac{cos(Mw_c)-\delta_{comp}}{\cos(Kw_c)-1} \quad (8)$$

where $\delta_{comp} = \frac{1}{\delta_c}$ and δ_c should be less than $0.01\ dB$. If the passband droop is within the desired limit, then the transfer function of compensated filter can represented in canonical signed digit (CSD) as:

$$H_{comp-CSD}(z^K) = x_{CSD} + y_{CSD}z^{-K} + x_{CSD}z^{-2K} \quad (9)$$

where x_{CSD} *and* y_{CSD} are the CSD representations of the quantized coefficients x_q *and* y_q of the proposed compensation filter that satisfied the relation $2x_q + y_q = 1$ and given by-

$$x_q = 2^{-p}\left(\frac{v}{2^{-p}}\right) \quad (10)$$

$$y_q = 2^{-p}\left(\frac{u}{2^{-p}}\right) \quad (11)$$

The procedure is continued until the desired Pass band compensation is obtained. There is a tradeoff between the desired compensation of the pass band droop and filter coefficients can control the desired pass band droop of the overall decimation filter.

V. Design Issue and Performance Analysis

In narrowband applications, where decimation rates are very high, an efficient decimation filters such as the CIC filter is needed to reduce the signal to its baseband [15]. The CIC decimation filter has a poor low bass response, however, they are easy to implement and not require multiplications in real-time. Low pass magnitude response can be improved by compensating the passband droop with FIR filter. For a CIC decimator, the compensation filter operates at the decimated sample rate and provides $(x/sin(x))^P$ shaping. The CIC data path undergoes internal register growth that is a function of all the design parameters: P, K in addition to the input sample precision S.

$$S_{max} = \lceil Plog_2 K + S - 1 \rceil \quad (12)$$

The cascade equivalence is used to build an efficient compensated CIC decimation filter structure. Fig. 3 shows the uncompensated CIC frequency response, the compensation filter frequency response and Overall response of compensated CIC with polyphase structure.

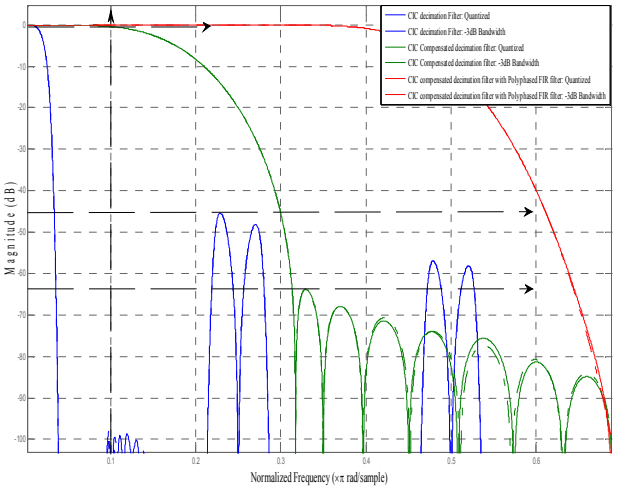


Fig. 3 (a) Overall Magnitude Response for decimation factor 64

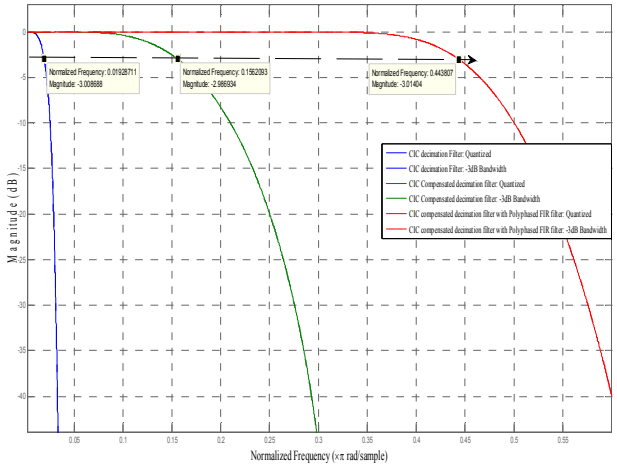


Fig. 3 (b) Passband details (-3dB down): Zoom View

TABLE I
Passband-Droop Compensation Chart

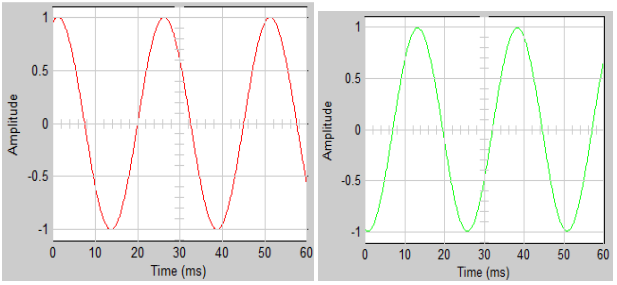
Filter Stages with decimation Factor (D) = 64	Magnitude (dB) of Passband droop at Normalized Frequency ($\times \pi \frac{rad}{sample}$)							
	0.02	0.1	0.15	0.20	0.25	0.30	0.4	0.45
CIC decimation Filter	-3.517	---	---	---	---	---	---	---
CIC Compensation Filter	7.89e-009	-0.368	-2.494	-8.317	-19.953	-45.5	-84.31	-97.39
Compensated CIC Polyphased Decimation filter	7.88e-009	4.8e-008	-5.21e-008	-7.156e-008	-2.03e-008	-0.003	-0.811	-3.552

TABLE II
COMPARATIVE CHART OF HARDWARE COMPLEXITY OF DIFFERENT DECIMATION FILTER STRUCTURES

Number of Section = 2	Distributed Decimation Filter	CIC Decimation Filter	FIR Decimation Filter	Multirate Compensated CIC Filter
Decimator Factor	8*4*2	64	64	8*4*2=64
Number of Multipliers	103	0	1265	103
Number of Adders	105	4	1264	105
Number of States	102	4	1216	102
Multiplications per Input Sample (ns)	38.5	0	19.7656	2.4219
Additions per Input Sample (ns)	40	2.313	19.75	4.625

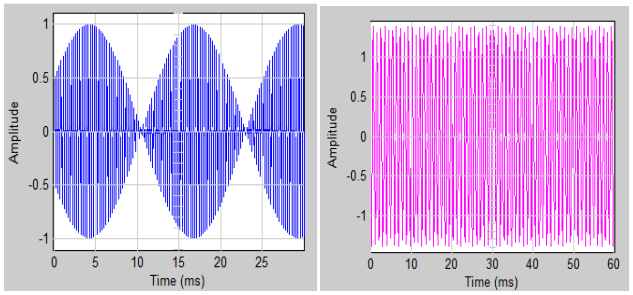
We have done the performance analysis on the basis of two factors: (a) Use of Compensated CIC filter in narrow band filtering to get the unaltered desired output with high yield and (b) Hardware complexity (i.e. No. of adders and multipliers) with high speed down sampling.

Tables I & II and Figs. 3-5 demonstrate the different responses generated by multirate FIR decimator and CIC compensator along with passband droop compensation chart. The initially CIC decimation filter having a large passband droop i.e. 3.517 dB at $0.02\,\pi\frac{rad}{sample}$ without any compensation method and getting even more worst in high frequencies. CIC decimation filter with FIR compensation introduce a significant improvement in its passband characteristic as shown in Fig. 3. Compensated CIC decimation filter with FIR compensation and polyphased FIR compensation improves the passband droop by 1.97% and 25.57% respectively, and hence the passband droop is compensated by a significant amount to get a desirable flat lowpass characteristic. It is also observed that the output response of the original transmitted signal is unaltered in compensated CIC filter w.r.t. FIR filter, but it also deals a great improvement in terms of its speed and area. Through the proper analysis (Table II), it is found that the CIC compensator filter uses much lesser no. of adders and multiplier than FIR filter with comparable filter lengths as it utilizes conventional CIC filter which is having a multiplierless internal structure.



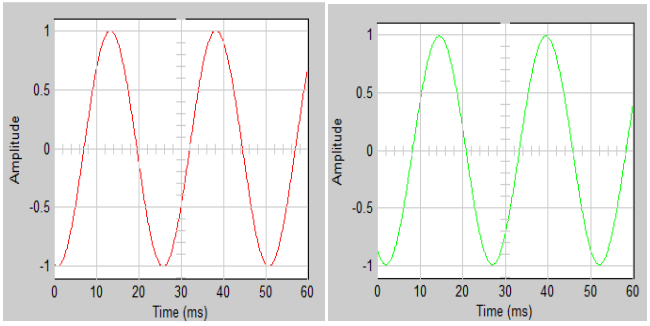
(i) Original Signal (ii) Low Pass

Fig. 4 (a) Three stages multirate Narrowband Filtering Using FIR Filter



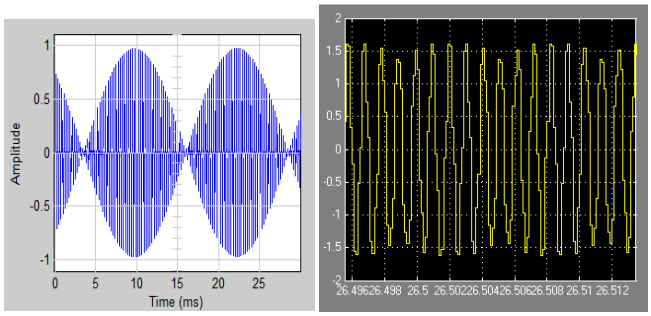
(iii) High Pass (iv) Band Pass

Fig. 4 (b) Three stages multirate Narrowband Filtering Using FIR Filter



(i) Original Signal (ii) Low Pass

Fig. 5 (a) Three stage multirate Narrowband Filtering Using CIC Compensator Filtering



(iii) High Pass (iv) Band Pass

Fig. 5 (b) Three stage multirate Narrowband Filtering Using CIC Compensator Filtering

VI. RESULT ANALYSIS

After the proper analysis and comparison of compensated CIC filter structure with FIR filter, it is found that the output response of compensated CIC filter is not only unaltered, but

also deals a great improvement in terms of its passband droop, speed and area in narrow band application. It is also observed that the Compensated CIC decimation filter with FIR compensation improves the passband droop by 25.57% and to get the same response, FIR filter utilizing 1265 no. of multiplier, 1264 no. of adder, 19.7656ns multiplications per input sample (MPIS) and 19.75ns additions per input sample (APIS) w.r.t. 103 no. of multiplier, 105 no. of adder, 2.4219ns multiplications per input sample (MPIS) and 4.625ns additions per input sample (APIS) respectively, using CIC compensator filters and hence the overall response time is reduced by 12.25% MPIS and 23.4% APIS respectively w.r.t. FIR filter. This proposed structure shows a significant improvement in terms of its hardware complexity and hence its down sampling speed is also improved w.r.t FIR filter structure. This compensated filter structure with polyphase decomposition is more efficient in terms of the desired passband droop of the overall decimation factor, response time and hardware complexity, but the width of the passband and the frequency characteristics outside the passband are severely limited due to passband aliasing or imaging error. Pecotic, M. G. et al. [18] presented a method for the design of finite-impulse-response CIC compensators whose coefficients are expressed as the sums of powers of two (SPT) based on the minimax error criterion to improve these characteristics. Recently, the paper [19] presents a double sharpened CIC decimation filter to compensate the narrow passband droop and to achieve better stop band alias rejection.

VII. Discussion and Conclusion

The computational efficiency of multirate algorithms is based on the ability to use simultaneously different sampling rates in the different parts of the system. The decimation of a signal at high frequency using FIR or IIR structures is very complex since it needs a lot of multiplications and hence the system cost is increased. This paper presents hardware efficient compensated CIC filter over a narrow band frequency that increases the speed of down sampling by cascading different stages of CIC and FIR filters. In CIC filter as the number of stages increases its stop band attenuation improves, but pass band droop increases, whereas the FIR filters provide the desired passband transition characteristics. The CIC compensator filters are more efficient to have the same response for required signals than those from FIR decimation and interpolation filters in multiple stages. The filter length reduces up to 75% with a reduction in the number of multipliers from 93.6% to 98.8%. Multiplication per input sample and addition per input sample reduces to 12.25% and 23.4% respectively. This results in hardware efficiency of the CIC compensator filters.

Acknowledgment

This work was supported by the Gautam Buddha Technical University (GBTU) and Harcourt Butler Technological Institute (H.B.T.I.) in the research field of Electronics Engineering.

References

[1] E. B. Hogenauer, "An Economical Class of Digital Filters for Decimation and Interpolation", *IEEE Trans. on Acoustics, Speech, and Signal Processing*, Vol. ASSP-29, pp. 155-162, April 1981.

[2] Gustafsson, O., Johansson, H. and Wanhammar, L. "Narrow-band and wideband single filter frequency masking FIR filters, "IEEE International Symposium on Circuits and Systems ISCAS 2001, vol. 2, pp. 181-184, may 2001.

[3] J. Kwentus, Z. Jiang, and A. N. Willson, Jr., "Application of filter sharpening to cascaded Integrator-comb decimation filters," IEEE Transactions on Signal Processing, Vol. 45, pp. 457-467, February 1997.

[4] Lyons, R." Interpolated narrowband lowpass FIR filters," IEEE Signal Processing Magazine, vol. 20, Issue 1, pp. 50-57, Jan. 2003.

[5] Rabiner, L. and Crochiere, R. " A novel implementation for narrow-band FIR digital filters," IEEE Trans. on Acoustics, Speech and Signal Processing, vol. 23, Issue 5, pp. 457-464, 1975.

[6] G. Jovanovic-Dolecek and S. K. Mitra, "Sharpened comb decimator with improved magnitude response," Proc. 2004 International Conference on Acoustics, Speech, and Signal Processing, Montreal, Canada, Proc. Vol. 2, pp. 393-396, May 2004.

[7] Kayano, H., Kawaguchi, T., Shiokawa, N., Nakayama, K., Watanabe, T. and Hashimoto, T. "Narrow-Band Filter for Transmitter of Radar Application," 38th European Microwave Conference, EuMC 2008, pp. 853-856, Oct. 2008.

[8] Saramaki, T. and Mitra, S.K. " Design and implementation of narrow-band linear-phase FIR filters with piecewise polynomial impulse response," Proceedings of IEEE International Symposium on Circuits and Systems, ISCAS '99, vol. 3, pp. 456-461, July 1999.

[9] Lehto, R., Saramaki, T. and Vainio, O. " Synthesis of Narrowband Linear-Phase FIR Filters With a Piecewise-Polynomial Impulse Response," IEEE Transactions on Circuits and Systems, vol. 54, Issue 10, pp. 2262-2276, Oct. 2007.

[10] G. Jovanovic-Dolecek and S. K. Mitra, " Efficient multistage comb-modified rotated sinc (RS) decimator,"Proc. EUSPCO-2004, Vienna, Austria, pp.1425-1427, September, 2004.

[11] Gordana J. Dolecek and Fernando J. Trejo Torres,"Compensated CIC-Cosine Decimation Filter " ECTI Trans. on Computer And Information Technology Vol.4, No.1, pp. 8-13, May 2010.

[12] Neuvo, Y., Rajan, G. and Mitra, S. " Design of narrow-band FIR bandpass digital filters with reduced arithmetic complexity," IEEE Transactions on Circuits and Systems, vol. 34, Issue 4, pp. 409-419, April 1987.

[13] Swanson, D.G., Tyco Electron. and Lowell "Narrow-band microwave filter design," IEEE Microwave Magazine, vol. 8, Issue 5, pp. 105-114, Oct. 2007.

[14] G. Jovanovic Dolecek and S.K. Mitra "Two-stage CIC-based decimator with improved characteristics",IET Signal Processing, INAOE, Los Angeles, USA.,Volume 4, 1, pp.22–29, 2010.

[15] Xiangkun Chen and Parks, T. " Analytic design of optimal FIR narrow-band filters using Zolotarev polynomials,"IEEE Transactions on Circuits and Systems, vol. 33, Issue 11, pp. 1065-1071, Nov. 1986.

[16] G. J. Dolecek and Fred Harris, "Design of wideband CIC compensator filter for a digital IF receiver", Digital Signal Processing 19, ELSEVIER, pp. 827–837, April, 2009

[17] Dolecek, G.J., Carmona, J.D. "Generalized CIC-cosine decimation filter", IEEE Symposium on Industrial Electronics & Applications (ISIEA), Mexico, pp. 640-645, 3-5 Oct. 2010

[18] Pecotic, M.G., Molnar, G. , Vucic, M. "Design of CIC compensators with SPT coefficients based on interval analysis", Proceedings of the 35th International Convention MIPRO, Croatia, pp. 123-128, 21-25 May 2012.

[19] P. Durai Saravanan, "Design and Implementation of Efficient CIC Filter Structure for Decimation", International Journal of Computer Applications, pp.1-7, Volume 65(14), March 2013

Mr. Vishal Awasthi received his B.E. and M. Tech. degree in the field of Electronics & Communication Engineering from Mumbai University and HBTI, Kanpur in 1999 and 2007 respectively. His area of interest is Digital signal processing and Control system. Presently he is working as incharge of the Department of Electronics & Communication Engineering, UIET, C.S.J.M. University, Kanpur (UP), India.

Dr. Krishna Raj has completed his Ph.D. in the field of Computer Arithmetics. He is a Fellow Member of IETE and working as Associate Professor in the Department of Electronics Engineering, H.B.T.I. Kanpur. His Area of interest is Digital Signal Processing and Computer Arithmetic.