3D Quantum Numerical Simulation of Horizontal Rectangular Dual Metal Gate\Gate All Around MOSFETs

M. Khaouani, A. Guen-Bouazza, B. Bouazza, Z. Kourdi

Abstract—The integrity and issues related to electrostatic performance associated with scaling Si MOSFET bulk sub 10nm channel length promotes research in new device architectures such as SOI, double gate and GAA MOSFET. In this paper, we present some novel characteristic of horizontal rectangular gate\gate all around MOSFETs with dual metal of gate we obtained using SILVACO TCAD tools. We will also exhibit some simulation results we obtained relating to the influence of some parameters variation on our structure, that having a direct impact on their threshold voltage and drain current. In addition, our TFET showed reasonable I_{ON}/I_{OFF} ratio of (10^4) and low drain induced barrier lowering (DIBL) of 39 mV/V.

Keywords—GAA, SILVACO, QUANTUM, MOSFETs.

I. INTRODUCTION

IN metal-oxide semiconductor field-effect transistor (MOSFET) the limiting of scaling in many new device structures are widely explored on approach [1]. Among them, gate-all-around MOSFET is attractive for the following reasons: its immunity to short channel effects, drain induced barrier lowering, handling out of the gate, and the reduction of leakage current [2], and are promising candidate's future CMOS devices due to their reduced short-channel effects [3]. The effects of quantum mechanics have been included in several books related to the square GAA JLFETs [4], [5], but none of quantum effects has been modeled in extremely devices - scale where quantum confinement effects become important and governing the performance of the device. The GAA MOSFET, which is basically a 3-D structure, cannot be analyzes directly the same way. One possibility is to solve Laplace's equation in rectangular coordinates by means of a series expansion in Bessel functions [6]. And used in simulation Bohm quantum potential (BQP) model calculate a position dependent potential energy term using an auxiliary equation derived from the Bohm interpretation of quantum mechanics. This extra concentration is integrated in the whole structure and then this quantity is derived as C=-dQ/dV [7].

In this paper we have performed 3D quantum numerical simulation of horizontal rectangular dual metal gate \gate all around MOSFET using SILVACO TCAD Tools an d present some interesting characteristics and the influence of some parameters variation on our Structure that having a direct impact on their drain current.

II. METHODOLOGY

The 3D structure obtained using ATLAS3D in SILVACO TCAD tools in Fig. 1, with L_G= 9nm, Tox= 1nm and W= H= 5nm, channel doping is 1E17cm^{-3}, drain and source doping concentration is 1E20cm^{-3} and used dual metal gate Aluminum (φ_{M1} = 4.1 eV) and Titanium (φ_{M1} = 4.4 eV).
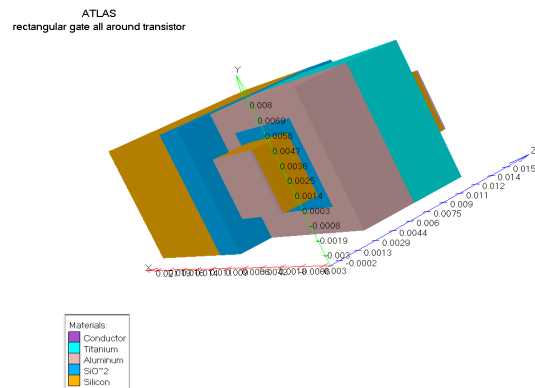

Fig. 1 3D View of rectangular dual metal gate \gate all around MOSFETs

The device has been simulated using ATLAS 3D for obtained output and transfer characteristics.

III. NUMERICAL ANALYSIS

Numerical simulation is an extremely helpful tool for detailed investigation of physical phenomena, which determine electrical characteristics of semiconductor devices. Simulation results we present in this study had been obtained using Atlas Silvaco Software [8].

M. Khaouani, A. Guen, Z. Kourdi, and B. Bouazza are with Electronique Departement, University of Tlemcen Research Unit of Materials and Renewable Energies, Algeria (e-mail: kh.3eln@live.3eln, guenbouazza@ yahoo.fr, zkourdi@hotmail.fr, benyounes@live.fr).

World Academy of Science, Engineering and Technology
International Journal of Electronics and Communication Engineering
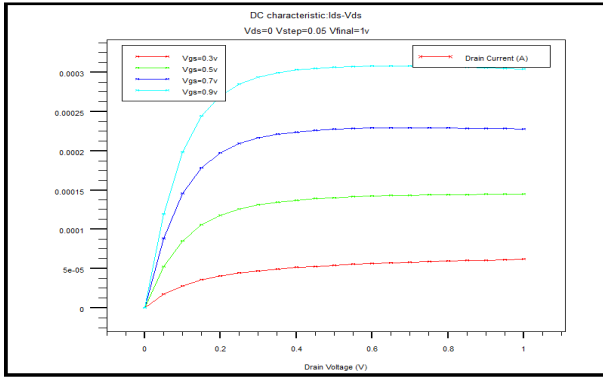Vol:8, No:4, 2014

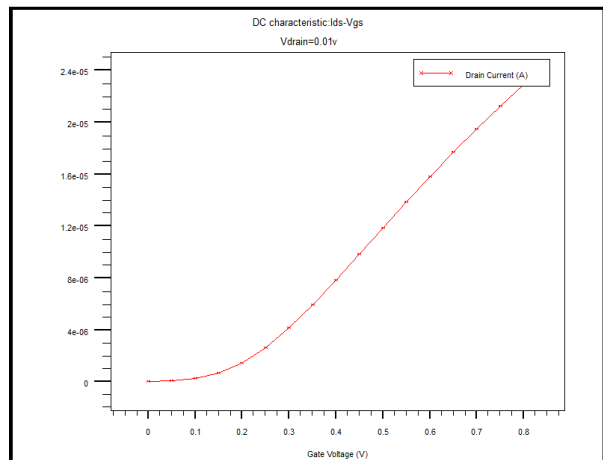Fig. 2 Simulated Output characteristics of dual metal gate GAA MOSFETs

Fig. 3 Simulated transfer characteristics for dual metal gate GAA MOSFETs.

Fig. 3 presents a transfer characteristics with a threshold voltage V_{TH}=120mv.

A. Influence of Parameters Variation on the Drain Current

In order to study the influence of our structure parameters such as oxide thickness, channel length and type of oxide with high-k dielectric like Si_3N_4, HFO_2 and thickness of metal on its electrical characteristics, some parameters are modified. We examine then the effect of their variation on the considered structure drain current.

1. Influence of Tox Variation I_D Courant and Threshold Voltage V_{TH}

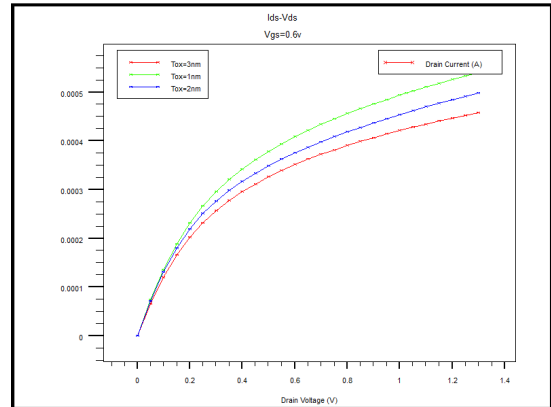Fig. 4 Output characteristics for a dual metal gate GAA MOSFETs at different oxide thickness (Tox=1nm, 2nm and 3nm)
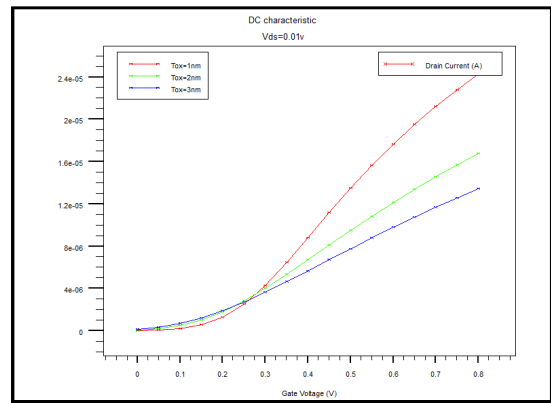

Fig. 5 Transfer characteristics for a dual metal gate GAA MOSFETs at different oxide thickness (Tox=1nm, 2nm and 3nm)

Fig. 4 illustrates characteristics for a GAA with dual metal gate MOSFET at different oxide thickness. At shorter oxide thickness, the drain saturation current increases strongly. We can conclude for this variation that thinner gate oxides lead to product higher drain currents. And in transfer characteristics in Fig. 5 if augment oxide thickness the threshold voltage reduce.

2. Influence Channel Length (L_{ch}) Variation ID Courant and Threshold Voltage V_{TH}

This section deals with the study of channel length variation effect on the electrical device characteristics.
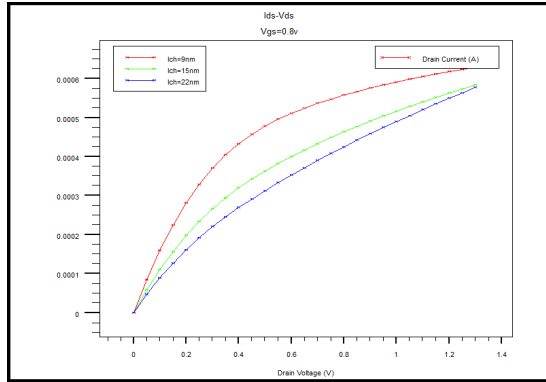
World Academy of Science, Engineering and Technology
International Journal of Electronics and Communication Engineering
Vol:8, No:4, 2014

Fig. 6 Output characteristics for a dual metal gate GAA MOSFETs at different oxide thickness (Lch=9nm, 15nm and 22nm)

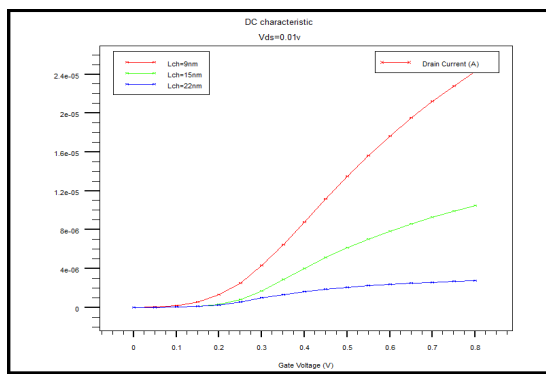Fig. 7 Transfer characteristics for a dual metal gate GAA MOSFETs at different oxide thickness (Lch=9nm, 15nm and 22nm)

In Fig. 6 that when in reduce L_{ch} the drain currents augment and in Fig. 7 when in reduce Lch the threshold voltage reduce. We can conclude that the reduce of the length of the cannel gives a very good drain current.

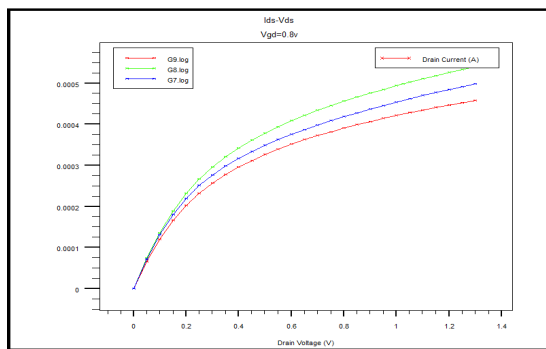3. Influence Channel Doping Dual Metal Gate GAA MOSFETs Variation ID Courant and Threshold Voltage VTH

Fig. 8 Output characteristics for a dual metal gate GAA MOSFETs at different ND (ND=1x1017 cm-3,1x1018 cm-3 and 1x1019 cm-3)
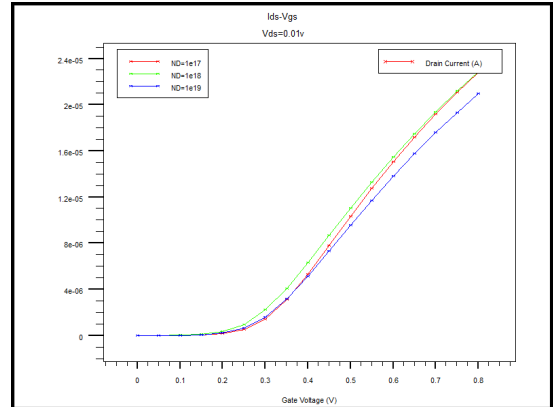

Fig. 9 Transfer characteristics for a dual metal gate GAA MOSFETs at different ND (ND=1017 cm-3, 1018 cm-3and 1019cm-3)

We note that in Figs. 8 and 9 with $N_D=10^{18}$ cm^{-3} doping the drain current augment and threshold voltage reduce.

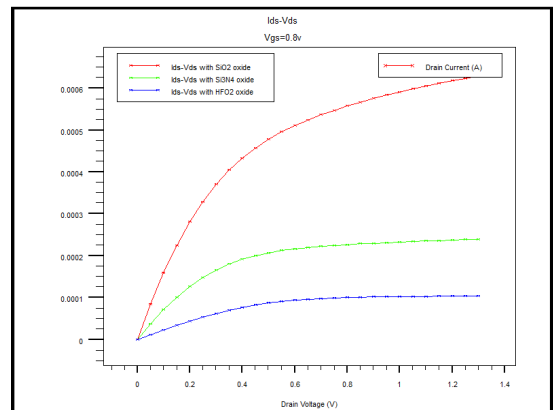4. Influence Type Oxide Variation ID Courant and Threshold Voltage V_{TH}

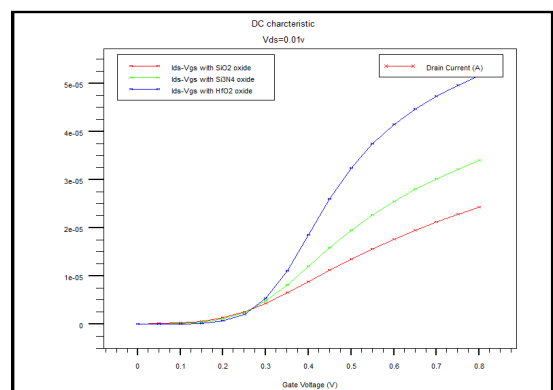Fig. 10 Output characteristics for a dual metal gate GAA MOSFETs at different type oxide (SiO2, Si3N4, HFO2)

Fig. 11 Transfer characteristics for a dual metal gate GAA MOSFETs at different type oxide (SiO2, Si3N4, HFO2)

In Figs. 10 and 11 the drain current augment and the voltage threshold voltage reduce with the SiO_2 oxide de grille.

DIBL (Drain Induced Barrier Lowering) Ion/Ioff Ratio

World Academy of Science, Engineering and Technology
International Journal of Electronics and Communication Engineering
Vol:8, No:4, 2014

The DIBL (Drain Induced Barrier Lowering) piercing said phenomenon which occurs when the dimensions of defected areas (ZCE) source / substrate and drain / substrate become comparable to the length of the grid. The potential distribution in the channel then depends on both the transverse field (controlled by the gate voltage), but also the longitudinal field (controlled by the drain voltage) than increase in the drain side ZCE, which causes the lowering of the barrier of source / substrate potential.
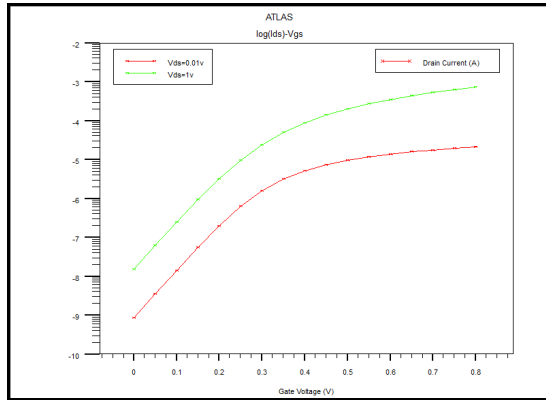

Fig. 12 Characteristics for a dual metal gate GAA MOSFETs

The DIBL effect is usually measured by the offset of the transfer curve in plan as the threshold divided by ΔV_{TH} and ΔV_D between two resulting curves of two different drain voltages:

$$DIBL = \frac{\Delta V_{TH}}{\Delta V_D}(mV/V) \qquad (1)$$
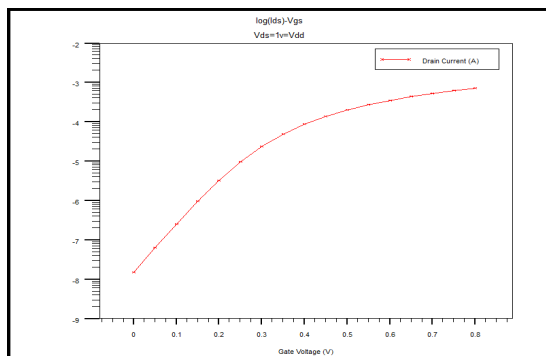
From (1) and Fig. 12 has DIBL=39mV.

Fig. 13 Characteristics for a dual metal gate GAA MOSFETs

From the Fig. 13 the reasonable I_{ON}/I_{OFF} ratio has (10^4).

IV. CONCLUSION

The downward revision of bulk planar MOSFET according to the International Technology Roadmap sheet for Semiconductors ITRS requires new structures such as MOSFETs gate all around (GAA MOSFETs). These structures can reduce short channel effects that appear below 10nm node. GAA MOSFETs structure that we study is a horizontal rectangular GAA MOSFETs with different type of metal in the grid and made the variation The variation of individual parameters of the structure were performed to calculate their effect on the characteristics of the device. Based on the simulation results we have obtained using the SILVACO software, we can choose the appropriate parameters for the optimization of our structure, with good reduction of short channel effects.

REFERENCES

[1] The International Technology Roadmap for Semiconductors (ITRS), 2012.
[2] S. D. Suk, S.-Y. Lee, S.-M. Kim, E.-J. Yoon, M.-S. Kim, M. Li, C. W. Oh, K. H. Yeo, S. H. Kim, D.-S. Shin, K.-H. Lee, H. S. Park, J. N. Han, C. J. Park, J.-B. Park, D.-W. Kim, D. Park, and B.-I. Ryu, "High performance 5 nm radius twin silicon nanowire MOSFET (TSN).
[3] J.-T. Park et al., IEEE Trans. Elec. Dev., 49(12), p.22
[4] Martinez , A. Brown, S. Roy, and A. Asenov , " Negf simulations of a junctionless if gate -all-around nanowire transistor with discrete dopants, "in Ultimate Integration on Silicon (ULIS)2011 12th International Conference on, P. 1-4 , IEEE , 2011.
[5] P. Razavi , G. Fagas , I. Ferain , N. Akhavan , R. Yu, and J. Colinge , "Performance investigation of junctionless Multigate short -channel transistors , "in Ultimate Integration on Silicon (ULIS), 201112th International Conference on, P. 1-3 , IEEE , 2011.WFET): Fabrication on bulk Si wafer, characteristics, and reliability," IEDM Tech. Dig., 2005, pp. 717720.
[6] H. A. El Hamid, B. Iñiguez, and J. Roig, "Analytical model of the threshold voltage and subthreshold swing of undoped cylindrical gate-allaround-based MOSFETs," IEEE Trans. Electron Devices, vol. 54, no. 3, pp. 572–579, Mar. 2007.
[7] G. Iannaccone, G. Curatola, G. Fiori, "Effective Bohm Quantum Potential for device simulators based on drift diffusion and energy transport", Simu- lation of Semiconductor Processes and Devices 2004, vol. 2004, pp. 275 -278, Sept. 2004.
[8] SILVACO, ATLAS User's Manual, Ver. 4.0, June 1995