World Academy of Science, Engineering and Technology
International Journal of Energy and Power Engineering
Vol:8, No:7, 2014

The Design of PFM Mode DC-DC Converter with DT-CMOS Switch

Jae-Chang Kwak, Yong-Seo Koo

***Abstract*—**The high efficiency power management IC (PMIC) with switching device is presented in this paper. PMIC is controlled with PFM control method in order to have high power efficiency at high current level. Dynamic Threshold voltage CMOS (DT-CMOS) with low on-resistance is designed to decrease conduction loss. The threshold voltage of DT-CMOS drops as the gate voltage increase, resulting in a much higher current handling capability than standard MOSFET. PFM control circuits consist of a generator, AND gate and comparator. The generator is made to have 1.2MHz oscillation voltage. The DC-DC converter based on PFM control circuit and low on-resistance switching device is presented in this paper.

***Keywords*—**DT-CMOS, PMIC, PFM, DC-DC converter.

I. Introduction

RECENTLY, the importance for power management IC(PMIC) is emphasized as battery-powered portable electronics such as smart phone are commonly used. In addition, research and development on high efficiency is essential to maximize the use of portable device that are preferred various functions than in the past. PMIC for high efficiency usually change drastically from linear regulator to switching regulator. But the switching regulator have disadvantage of low efficiency compared with linear regulator at light load conditions. Therefore, this paper is presented the using of switching regulator at heavy load conditions.

All power supply device of Mobile appliance must be made stable and various DC output voltage of high effectiveness from a unstable DC input power supply. For that reason, it is used do a power supply of Switched Mode Power Supply (SMPS) method instead of a power supply of conventional linear method.

Therefore, in this paper, DC-DC converter for power supplies is designed using DT-CMOS which is low on-resistance than CMOS.

II. DT-CMOS (Dynamic Threshold Voltage MOSFET)

A. What Is DT-CMOS?

Switching loss is fixed cause, but conduction loss by on -resistance of switch is increased by a output current increased.

Jae-Chang Kwak is with Department of Computer Science, University of Seokyeong, 124 Seokyeong-ro, Seongbuk-gu, Seoul, Korea

Yong-Seo Koo is with the Department of Electronics & Electrical Engineering University of Dankook, 126 Jukjeon-dong, Suji-gu, Yongin-si, Gyeonggi-do, 448-701, Korea (Corresponding author, e-mail: yskoo@dankook.ac.kr)

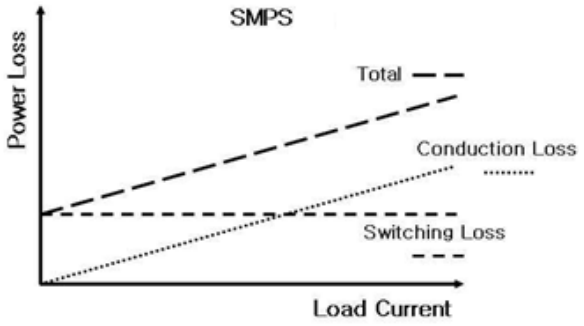

Fig. 1 Power loss analysis SMPS

When output current is increased, conduction loss is increased more than switching loss in high output current as shown in Fig. 1.

Finally, switch development that have low on-resistance to heighten efficiency of SMPS is essential.

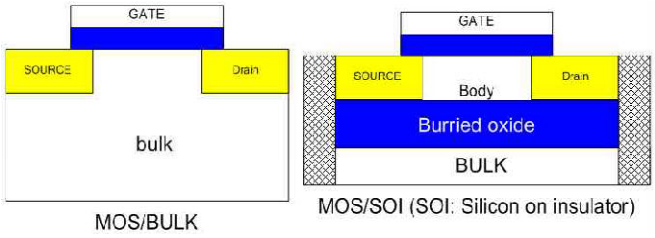

Fig. 2 CMOS and DT-CMOS (Dynamic Threshold voltage CMOS)

Dynamic Threshold voltage MOSFET (DTMOS) is designed by using SOI wafer as shown in Fig. 2. [1]

When the switch is became ON after connecting gate and p-substrate, heighten body voltage so that threshold voltage is lowered. When the switch is become OFF, the body is connected to the ground so that threshold voltage is heightened.

In this paper, we proposed available DT-CMOS without high leakage currents in high power supply voltages using this DT-CMOS's concept.

The proposed DT-CMOS in this paper can be seen in Fig. 3. When the switch is became ON, the body voltage of the switch MOS is controlled by diode connection CMOS and the threshold voltage is lowered. When the switch is became OFF, body of CMOS is connected to each the power supply and the ground.

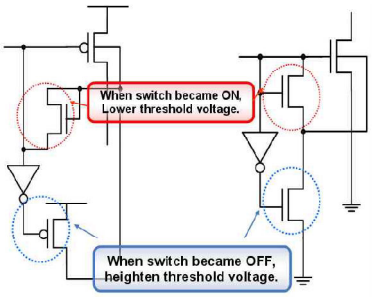

Fig. 3 Proposed DT-CMOS

When the switch is ON, the proposed DT-CMOS due to low threshold voltage is low on-resistance than conventional CMOS switches. Limitation of power supply voltage by the leakage current is overcame by minimizing body leakage current that is a conventional DT-CMOS fault through deciding supply and the ground.

In this paper, the DT-CMOS is designed with CMOS process on purpose to do one-chip of DT-CMOS and PFM control circuit. The DT-CMOS is designed with Deep-Nwell isolation from substrate and body to conventional silicon wafer as shown in Fig. 4. One-chip of switching device and PFM control circuit are designed by this technique.[2]

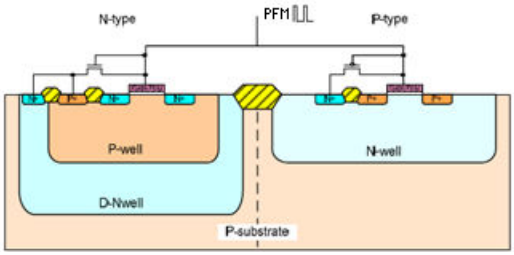

Fig. 4 The cross section of the proposed DT-CMOS

B. Characteristic Analysis of DT-CMOS Switch

In this paper, we compare threshold voltage and I-V characteristic of DT-CMOS with CMOS. The simulation circuit is designed as shown in Fig. 5.

When VDD is 3.3V input voltage, threshold voltage simulation is done by increasing VGS.

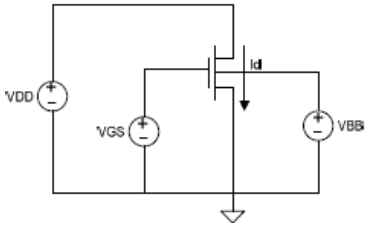

Fig. 5 Switching characteristic simulation circuit

Because of low threshold voltage, DT-CMOS is possible conduction of more current than CMOS in same voltage as shown in Fig. 6.

I-V characteristic simulation is done by increasing VDS. DT-CMOS is possible conduction of more current than CMOS in same voltage as shown in Fig. 7.

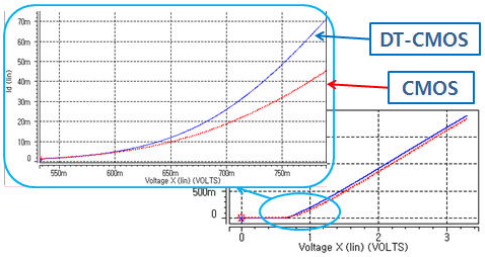

Fig. 6 Comparison of Threshold voltage

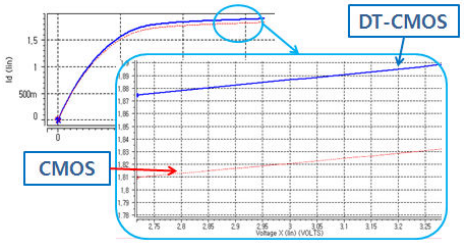

Fig. 7 Comparison of I-V characteristics

C. Efficiency Analysis of DT-CMOS Switch

We compare DT-CMOS with conventional CMOS as buck converter simulation. The simulation circuit is designed as shown in Fig. 8.

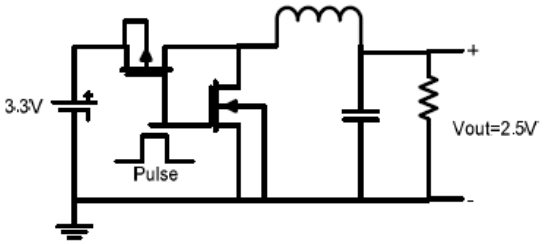

Fig. 8 Buck converter

We change load current and compare efficiency for comparing efficiency of DT-CMOS and CMOS. When load current is changed from minimum 0.1mA to maximum 300mA, the efficiency of CMOS is higher until 10mA.But the efficiency of DT-CMOS is higher from 50mA as shown in Fig. 9.

When the output current of DC-DC converter is based on 100mA, the efficiency of CMOS is 96.25%, but the efficiency of DT-CMOS is 97%. If the efficiency of CMOS is 97%, the size of CMOS will be become double.

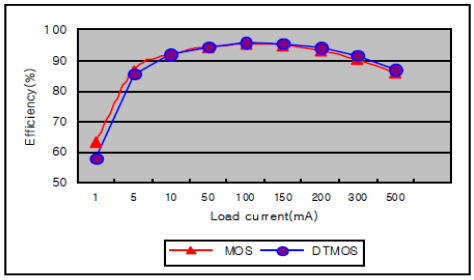

Fig. 9 DT-CMOS and CMOS efficiency by load current change

III. The Design of Proposed DC-DC Converter

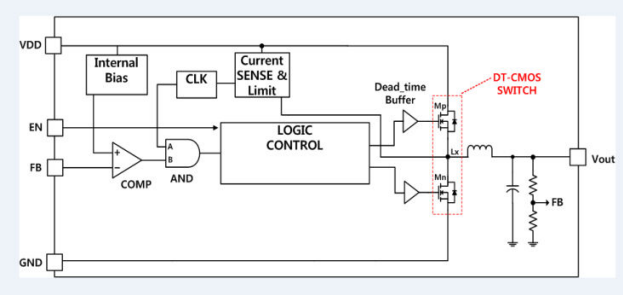

Fig. 10 DC-DC converter whole block diagram

Fig. 10 is function block diagram of the proposed buck converter. Proposed converter operates as PFM mode [3]. PFM waveform is applied to the gate of DT-CMOS switch, and ON-OFF of switch is determined. Thus the output voltage is formed. Feedback voltage formed by feedback resistor is formed output stage. The comparator generates a pulse by comparing the feedback voltage and reference voltage. Thus, pulses generated by comparator compared clock signal through AND gate. Finally, pulse generated by AND gate is applied to the low-side NMOS switch and high-side NMOS switch via the logic controller. It can be found through Fig. 11.

Low side switch is ON after the high side switches OFF and then low side switch is OFF before the high side switch ON for stable operation. It can be found through Fig. 12 [4], [5].

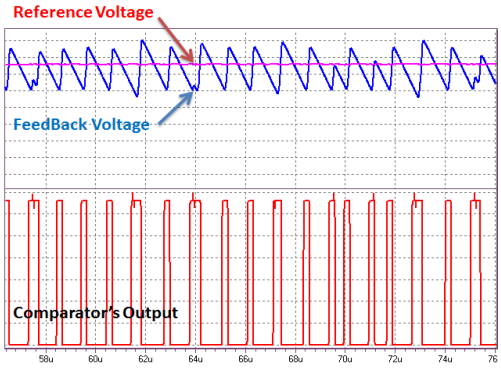

Fig. 11 Simulation result of PFM mode

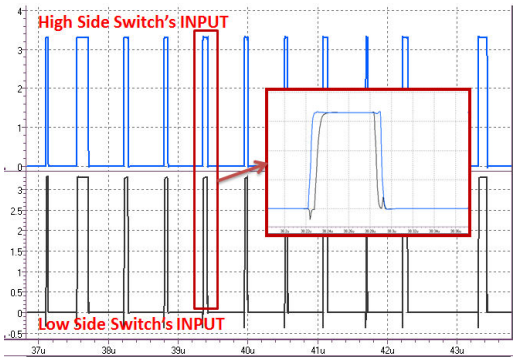

Fig. 12 Simulation result of switch's input

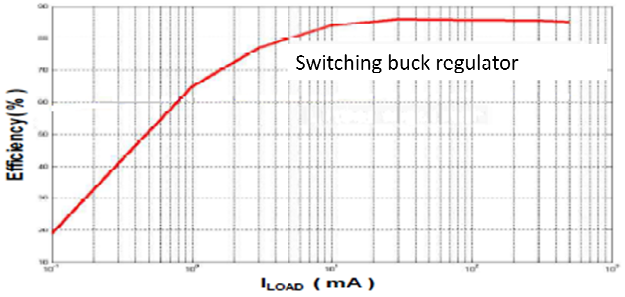

Fig. 13 Efficiency comparison of SMPS

SMPS of PFM method has high power conversion efficiency in high output current with that can be seen Fig. 13, but if output current becomes low, efficiency drops rapidly. Today portable terminals use fewer current in stand-by mode.

The PFM DC-DC converter that can be seen in Fig. 10 is designed using the PFM control circuit that is designed before. The performance of the DC-DC converter is a 3.3V input voltage, a 1.4V output voltage, maximum output current 100mA, a 1.2MHz switching frequency, maximum efficiency of 95% (inductor, capacitor ESR of 100mΩ), a 12mV ripple voltage. The efficiency of DT-CMOS is improved 0.5% than CMOS in the simulation result. Fig. 14 illustrates the inductor current, the inductor voltage, the output voltage of the DC-DC converter.

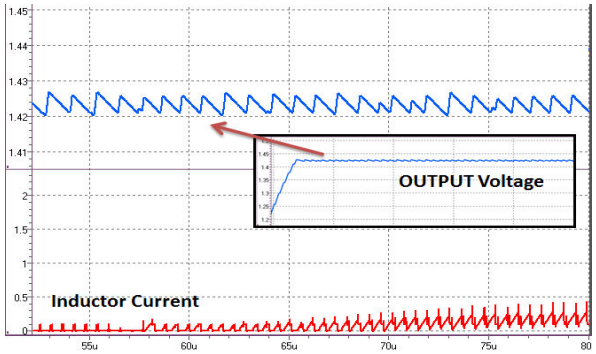

Fig. 14 Simulation result of DC-DC converter's output

IV. Conclusions

In this paper, the PFM Mode DC-DC converter that has low on-resistance switching elements are designed by using the DT-CMOS. High effectiveness for miniaturization and many long hours use is becoming a key issue in the DC-DC converter that is applied to portable terminal. Therefore, the proposed DC-DC converter heightened efficiency using the DT-CMOS instead of conventional CMOS and shortened size of a inductor that dominate the biggest area in the DC-DC converter using a switching frequency of 1.2MHz. The performance of the DC-DC converter is a 3.3V input voltage, a 1.4V output voltage, maximum output current 100mA, a 1.2MHz switching frequency, maximum efficiency of 95% (inductor, capacitor ESR of 100mΩ).

ACKNOWLEDGMENTS

This work was supported by the IT R&D program of MKE/KEIT [10035171, Development of High Voltage/Current Power Modules and ESD for BLDC Motors]. This research was supported by the MSIP (Ministry of Science, ICT & Future Planning), Korea, under University ITRC support program (NIPA-2014-H0301-14-1007) supervised by the NIPA (National IT Industry Promotion Agency).

REFERENCES

[1] Fariborz Assaderaghi, "A dynamic Threshold Voltage MOSFET for Ultra Low Voltage Operation", IEEE, 33.1.1p.
[2] R. Jacob Baker, "CMOS Circuit Design and Layout second edition," Wiley-inter science, pp. 613-900
[3] Lu Chen, "Design and Test of a Synchronous PWM switching Regulator System", IEEE 0-7803-6253-5(2000)
[4] A. Djemouai, "New CMOS Integrated Pulse Width Modulator for Voltage Conversion Applications", IEEE 0-7803-6542-9(2000)
[5] K. Mark Smith, Jr., "A Comparison of Voltage-Mode Soft-Switching Methods for PWM Converters ",IEEE Trans-Power Electronic, Vol. 12,No.2(1997)

Jae-Chang Kwak Jae-Chang Kwak was born in Seoul, Republic of Korea, in 1957. He received his B.S. in Computer Science of Yonsei University and M.S., Ph.D. in Computer Science from University of Iowa in 1983, 1989 and 1993, respectively. He joined the Department of Computer Science, Seokyeong University as a Professor, in 1995. His current research interests include Network Traffic Control, Real-time Scheduling, QoS, Embedded System

Yong-Seo Koo Yong-Seo Koo was born in Seoul, Republic of Korea, in 1957. He received his B.S., M.S. and Ph.D. in Electronic Engineering from Sogang University, Seoul, Republic of Korea, in 1981, 1983 and 1992, respectively. He joined the Department of Electronics and Electrical Engineering, Dankook University as a Professor, in 2009. His current research interests include semiconductor devices, such as power BJTs, LDMOSs, and IGBTs; high-efficiency power management integrated circuits (PMICs), such as DC-DC converters; and electrostatic discharge (ESD) protection circuit design.