Analysis of SCR-Based ESD Protection Circuit on Holding Voltage Characteristics

Yong Seo Koo, Jong Ho Nam, Yong Nam Choi, Dae Yeol Yoo, Jung Woo Han

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***Abstract*—**This paper presents a silicon controller rectifier (SCR) based ESD protection circuit for IC. The proposed ESD protection circuit has low trigger voltage and high holding voltage compared with conventional SCR ESD protection circuit. Electrical characteristics of the proposed ESD protection circuit are simulated and analyzed using TCAD simulator. The proposed ESD protection circuit verified effective low voltage ESD characteristics with low trigger voltage and high holding voltage.

***Keywords*—**ESD (Electro-Static Discharge), SCR (Silicon Controlled Rectifier), holding Voltage.

I. Introduction

THE development of semiconductor processing brought the increase of circuit speed and high-integration of integrated circuits. However, the malfunction and breakdown of circuits is being gradually acknowledged. Electrostatic discharge accounts for more than 70% of the destruction of the entire semiconductor integrated circuits [1]. For this reason, ESD has been considered as a major reliability threat in the semiconductor industry. As a process technology scales down, the design of ESD protection circuit becomes more challenging. To solve ESD problem, GGNMOS (Gate Grounded NMOS) and SCR (Silicon Controlled Rectifier) is commonly used in protection device. GGNMOS is easy to design and is perfectly compatible with CMOS processing. However, it consumes relatively large silicon area because of the low current driving capability. Hence, significant parasitic effects are present, which make GGNMOS devices the non-optimum solution for high ESD robustness, high frequency, large pincount, and area-sensitive IC chips [2]. SCR (Silicon Controlled Rectifier) which provide the high value of the area gain factor compare with other protection structures, is commonly used for ESD protection in advanced processes technology [3]-[6]. However, a SCR has high triggering voltage of approximately 20V compared to low holding voltage about 1~2V. When latch-up occurs by low holding voltage, it causes malfunction of internal circuit and destruction of gate oxide. In order to solve the latch-up problem due to the low holding voltage, adding to diode string or resistance of well is widely used [7].But these ways have problems that appear to increase the area of the ESD protection device and can increase the leakage current due to diode string [8].

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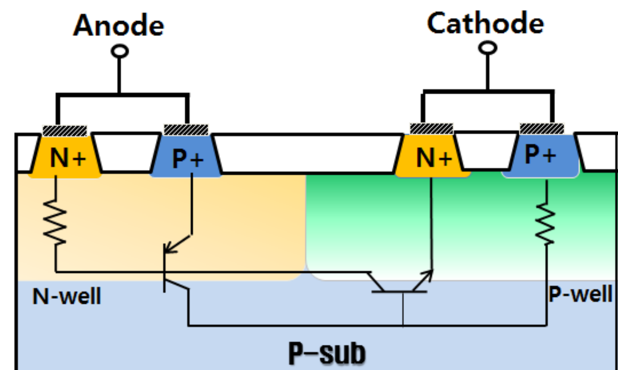
In this paper, for increasing the holding voltage, design parameters are set and the holding voltage characteristics are analyzed for design parameters.

II. The SCR Based ESD Protection Circuit

A. The Structure of the SCR-Based ESD Protection Circuit

The cross section of conventional SCR is shown in Fig. 1. When ESD surge is applied to SCR, potential of N-well increases. Eventually, N-well and P-well junction begin to avalanche because the high electric field crosses it, then EHP (Electron-Hole Pairs) are generated. Generated current makes voltage drop and NPN parasitic bipolar transistor turns on. After NPN transistor is turns on, its current makes PNP transistor turns on. Turned-on NPN/PNP transistors operate inlatch mode and it makes relatively low holding voltage about 2V.



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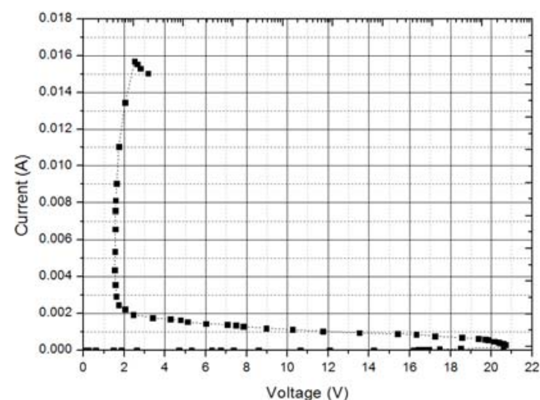

(b)

Fig. 1 Cross sectional view of conventional SCR (a) and simulation result (b)

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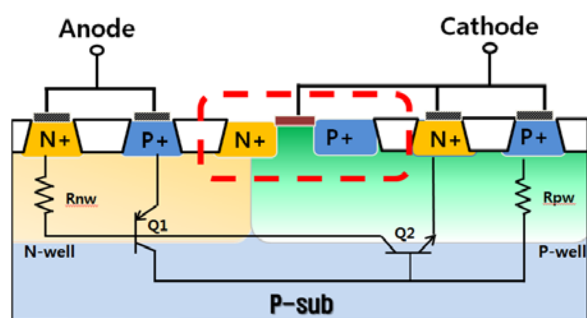
Fig. 2 shows cross sectional view and simulated I-V characteristic of the SCR-based ESD protection circuit. The P+ diffusion in the N-well forms the anode, and the n+diffusion in the p-sub forms the cathode of the SCR. And the SCR-based ESD protection circuit includes N+ bridge between N-well and P-well, P+ floating region and gate in the P-well. N+ bridge region of the SCR-based ESD protection circuit is inserted so that the breakdown will be initiated by an N+ bridge – P-well junction. P+ floating region in P-well increases holding voltage by reducing current gain of parasitic NPN bipolar transistor. The SCR-based ESD protection circuit has low trigger voltage and high holding voltage than conventional SCR.



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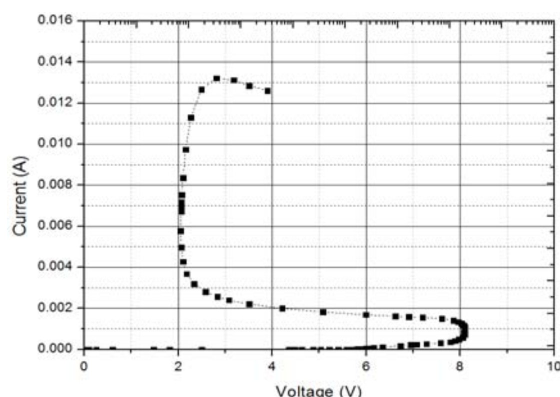

(b)

Fig. 2 Cross sectional view and simulated I-V characteristics ofthe SCR-based ESD protection circuit

TABLE I
SIMULATION RESULTS OF CONVENTIONAL SCR AND NOVEL SCR

Device	Trigger voltage	Holding voltage
Novel SCR	8.09V	2.05V
Conventional SCR	20.70V	1.56V

B. Operation of the SCR-Based ESD Protection Circuit

The operation of proposed SCR-based ESD protection circuit is as follows: The applied ESD pulse into anode makes high the potential of the N+ bridge between N-well and P-well. Then the N+ bridge and p-well junction becomes more reverse biased until it goes into avalanche breakdown. Avalanche breakdown generates EHP (Electron and Hole pair). And generated electron currents flow to N-well and hole currents flow to p-well. When potential of P-well is higher than potential of N+ cathode, the junction is forward-biased and parasitic NPN bipolar transistor (Q2) turns-on. When NPN bipolar transistor (Q2) turns-on, NPN bipolar transistor current generates a voltage drop across Rnwell and turns on the PNP bipolar transistor (Q1) as well. The current of the PNP bipolar transistor creates a voltage drop across Rpwell and helps to keep the NPN bipolar transistor. PNP bipolar transistor (Q1) and NPN bipolar transistor (Q2) operate in latch mode and discharge most of ESD current.

III. SIMULATION RESULTS AND ANALYSIS

To analyze holding voltage properties associated with design parameters, design parameters D1, D2, D3 have been set. Individual design parameters include gate length(D1) associated with base width of parasitic NPN bipolar transistor, a distance between P+ anode N+ bridge region(D2) and N+ floating region(D3) associated with base width of parasitic PNP bipolar transistor.

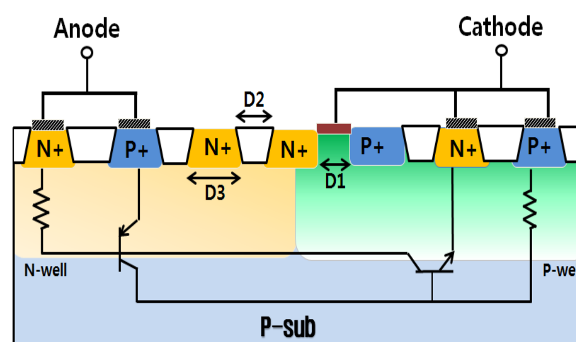

Fig. 3 Design parameters of SCR-based ESD protection circuit

The SCR-based ESD protection circuit is verified and compared by Synopsys TCAD simulator. As the gate length (D1) is increasing, current gain of parasitic NPN bipolar transistor is reduced and therefore holding voltage is increasing.

Fig. 4 (a) shows a graph when the design parameter D1 changes in length: 0.5um, 1um, 1.5um and 2um. The holding voltage is 2.05V, 2.13V, 2.20V and 2.24V respectively. Although fluctuation in holding voltage is not so much high as the length of gate increases, trigger voltage increases. The trigger voltage is increased because ESD discharge path increases between anode and cathode.

Fig. 4 (b) is a graph when a design parameter D2 is changed from 0.5um to 2um. The holding voltage is 2.05V, 2.12V, 2.25V and 2.33V respectively. A design parameter D2 is a distance between P+ anode and N+ bridge. As the length of D2 is increasing, the effective base width of parasitic PNP bipolar transistor (Q1) is extending. In other words, as D2 increases, the current gain for parasitic PNP bipolar transistor (Q1) is decreasing and the holding voltage of SCR is increasing.

Fig. 4 (c) is a graph when design parameter D3 is changed from 0um to 2um. As a design variable D3 is increasing in its length, the base width of parasitic PNP bipolar is increasing. Holding voltage is increased by approximately 1V from 2.26 to

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3.02V. But on-resistance is increased because of additional resistance in discharge path by D3 variables.

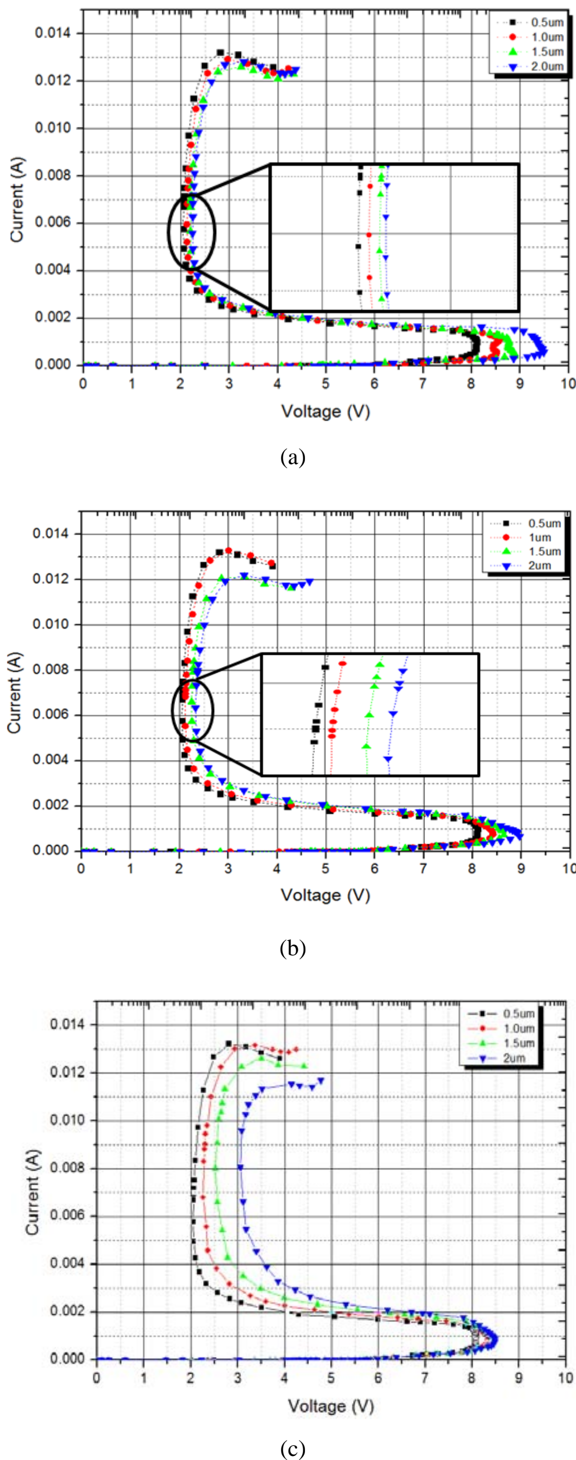

Fig. 4 Simulated I-V characteristics in variations in D1 (a), dD2 (b) and D3 (c) for the SCR-based ESD protection circuit

TABLE II
ELECTRICAL CHARACTERISTICS FOR EACH DESIGN VARIABLES FOR THE SCR-BASED ESD PROTECTION CIRCUIT

	Variation	Holding Voltage	Trigger Voltage
D1	0.5um	2.05V	8.10V
	1um	2.13V	8.48V
	1.5um	2.20V	8.86
	2um	2.24	9.46V
D2	0.5um	2.05V	8.10V
	1um	2.12V	8.39V
	1.5um	2.25V	8.60V
	2um	2.33V	8.96V
D3	0um	2.05V	8.10V
	1um	2..26V	8.29V
	1.5um	2.56V	8.38V
	2um	3.05V	8.47V

IV. CONCLUSION

This paper proposed SCR-based ESD protection circuit with reduced high trigger voltage based on structural change that has been a problem found at conventional SCR. Also, latch-up problem by increasing low holding voltage is improved. Electrical characteristics are analyzed through TCAD-medici simulation results. Trigger voltage for proposed circuit has been increased from 8.1V to maximum 9.46V as a design variables increases. Holding voltage is raised from 2.05V to 3.02V as design parameters increasing.

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