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Modelling and Simulation of Cascaded H-Bridge Multilevel Single Source Inverter Using PSIM

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***Abstract*—**Multilevel inverters such as flying capacitor, diode-clamped, and cascaded H-bridge inverters are very popular particularly in medium and high power applications. This paper focuses on a cascaded H-bridge module using a single direct current (DC) source in order to generate an 11-level output voltage. The noble approach reduces the number of switches and gate drivers, in comparison with a conventional method. The anticipated topology produces more accurate result with an isolation transformer at high switching frequency. Different modulation techniques can be used for the multilevel inverter, but this work features modulation techniques known as selective harmonic elimination (SHE).This modulation approach reduces the number of carriers with reduction in Switching Losses, Total Harmonic Distortion (THD), and thereby increasing Power Quality (PQ). Based on the simulation result obtained, it appears SHE has the ability to eliminate selected harmonics by chopping off the fundamental output component. The performance evaluation of the proposed cascaded multilevel inverter is performed using PSIM simulation package and THD of 0.94% is obtained.

***Keywords*—**Cascaded H-bridge Multilevel Inverter, Power Quality, Selective Harmonic Elimination.

I. Introduction

MULTILEVEL inverters are power-conversion systems composed of an array of power semiconductors switches and voltage or current sources, when properly connected and controlled, can generate waveform with variable and controlled frequency, phase, and amplitude [1]. To be called a multilevel inverter, each module phase has to produce at least minimum of three possible voltage level waveforms. A multilevel inverter has a practical approach for eliminating harmonics from the output voltage as different topologies and structures are mentioned in several literatures [2], [3]. Cascaded-bridge with proper configuration can vigorously operate many needed application such as residential, industrial, renewable energy interface, and electric vehicles [4].

Conventionally, each module of the inverter bridge contains "k" direct current (DC) voltage supply for 2k+1 levels to produce desired number of output voltage level [5]. The problem of voltage unbalance that occurs in conventional multilevel inverter, for the application that required long cable and multiple DC sources, will be overcome with the proposed topology. This work focuses on an H-bridge cascaded multilevel inverter that utilized a single DC voltage source, for its operation to enhance 11-level step voltage. The topology is advantageous for high to medium power applications because it supply sinusoidal voltage at higher switching frequencies with a low switching stress, and low total harmonic distortion (THD).

The multilevel inverters have several advantages as compared with 2-level inverters, such as the ability to operate at high voltage with lower voltage derivative per switching, higher efficiency and low electromagnetic interference [6]. To produce multilevel sinusoidal voltage output using single DC source, the semiconductor devices are to be triggered on and off in a pattern that the fundamental voltage is produced along with the elimination of certain desired number of higher order harmonics, so that low harmonic distortion in the alternating output voltage signal and power quality (PQ) are obtained. In order to switch the semiconductor devices for the inverter purpose, proper selection and configuration of switching angles are important factors, which directly affect the size and cost of the filter if any. The solution of transcendental nonlinear equations that characterized the harmonic component at fundamental or switching frequency are obtained and are referred to as selective harmonic elimination (SHE) equations [7].

As the SHE equations are nonlinear transcendental in form, their solutions consist of simple, multiple and even no roots for a particular value of the modulation index (M), as reported in numerous journals [8], [9]. Moreover, a big task is how to get all possible solution sets, where they exist by using simple and less complex method of computation. Iterative numerical methods have been implemented to solve the SHE equation generating only one solution set, and even for this, a proper initial guess and starting value of the modulation index for which the solution are required [9]. In fact, it is difficult to predict the initial solution and the modulation index value for which solution will be found and exist.

Traditional method to determine the switching angles with less complexity are proposed in [10]. When the switching pattern are obtained as required, the switching angles that will produce the lowest total harmonic distortion (THD), and power quality (PQ) in the voltage output waveform are selected for inverter switching [11].

Another important issue for the multilevel inverter is the more voltage steps, the less harmonic contents in its output. Increasing the number of steps in an inverter, not only result in additional number of components, but also result in a more complex control system of the inverter [2]. Therefore, it is a trade-off between voltage steps and complexity of the inverter control.

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II. Multilevel Inverter

In 1975 the multilevel inverters concept was introduced by Baker and Bannister [12]. The term multilevel inverter began with the three levels. Thereafter, numerous multilevel inverter configurations have been developed [2], [3].The primary idea and concept of a multilevel inverter was designed to achieve higher power, through operating a series power semiconductor switches with DC voltage sources to perform the power conversion by synthesizing a staircase voltage waveform as in Fig. 1. Multilevel inverter can be utilized several multiple or single DC sources for its operation, such as renewable energy, or batteries.

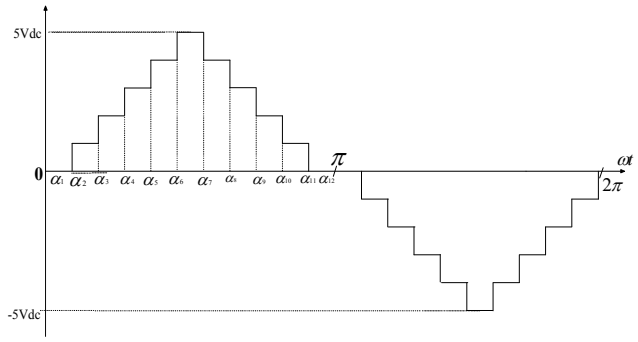

Fig. 1 Multilevel inverter waveform

A research work to improve high-voltage and high-current power semiconductors to drive high power systems still goes on. Earlier semiconductor devices collection are efficient to sustained high currents around 2.5 kA and voltages of 6.5 kV [3]. Presently, tough competition for the use of classic power inverter structure using high voltage semiconductors and new inverter topologies using medium voltage devices to level of 1 to 30 MW, and voltage of 34 kV [3]. Currently, multilevel inverters are in good shape for power applications solution, due to the fact that they can achieve high power using mature medium power semiconductor technology. The three basic multilevel inverter topologies are the neutral-point clamped inverter (NPC), flying capacitor inverter (FC), and cascaded H-bridge inverter (CHB) [13], [14]. These inverters can be classified as voltage source or current source inverters defending on its application.

Several research groups began to evolve the idea of increasing the voltage instead of the current. In order to achieve this objective, authors are developing new inverter topologies. As in [13], the first neutral point clamp (NPC) pulse width modulation (PWM) inverter (diode clamped) was presented.

Other multilevel inverter structures such as FC [15] and CHB [16] are of different properties and features as in the case with NPC, such as the modularity, control complexity, number of components, fault tolerance, and efficiency [2]. The inverter topology can be considered taking into account these factors for its applications. These factors make the multilevel inverters very popular and attractive to the academia and industry. Presently, researchers across the world are working continuously to improve multilevel inverter performances and efficiency, such as the control simplifications, and different optimization procedure, so that lowest THD output signals are obtained, for power quality system. Fig. 2 shows a conventional cascaded H-bridge multilevel inverter.

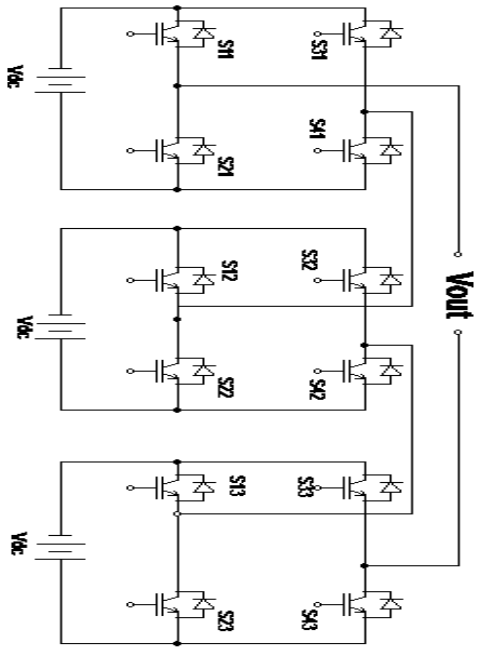

Fig. 2 Cascaded bridge multilevel inverter

A. Cascaded H-Bridge Module

The cascaded inverter proposed in this research consists of three parallel connected H-bridge modules, fed through a single DC supply. Two different topologies are considered for the simulation; the first case is without isolation transformer, while the second case is with isolation transformer. Each of the modules has four semiconductor switches and is configured such that it can generate a quasi-square voltage waveform (+E, 0, -E) at its output terminal. E is the main DC source from the supply unit. S_1, S_2, S_3 ...S_{12}, are the semiconductor switches. G_1, G_2, G_3 ....G_{12}, represent the gating signals used for controlling the MOSFETs on and off. Fig. 3 illustrates the proposed topology without isolation transformer.

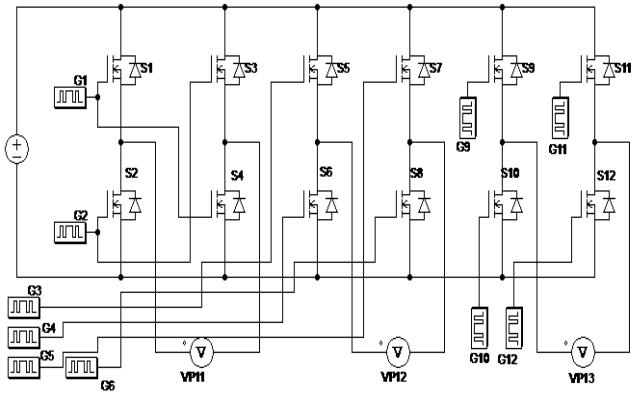

Fig. 3 Cascaded H-bridge without isolation transformer

VP_1, VP_2, and VP_3 are the voltage terminals of the respective bridges. The total voltage output for the inverter in Fig. 3 is given by;

$$v_{out} = vp_1 + vp_2 + vp_3 \quad (1)$$

The proposed system in Fig. 4 comprises of three transformers with series connected secondary side. Transformer 1 and 2 are designed to have 1:1 winding ratio, and transformer 3 to have 1:3 winding ratio, producing an output voltage across the load as expressed (2). The transformer not only provide isolation between the load and DC source, but also provide the means of increasing the number of output voltage step and quality signal waveform, without the need of additional inverter bridge or DC source. Equation (2) provides the total output voltage of the inverter in Fig. 4 below.

$$v_{out} = vp_1 + vp_2 + 3vp_3 \quad (2)$$

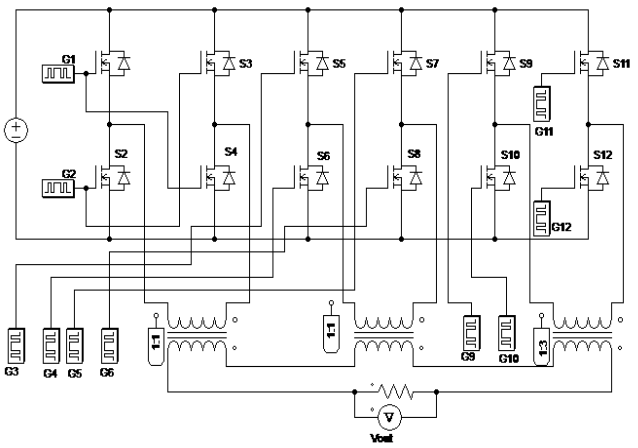

Fig. 4 Cascaded H-bridge with isolation transformer

The main advantages of the proposed topology are reduced number of switching devices and control complexity as compared with conventional multilevel inverter.

B. Switching Angle Analysis

The modulation technique employed on any kind of converter topology plays a major role in determining the properties of its output waveform [17]. Selective harmonic elimination approach is the modulation technique used in generating the 11-level of output voltage. Therefore, the switching angles need to be carefully selected, such that the intended desired odd harmonics are eliminated. This technique, apart from producing an output with a minimum total harmonic distortion THD, it also reduces the amount of electro-magnetic interference EMI and switching losses caused by high switching frequency [18], [19].

For a staircase waveform such as the one shown in Fig. 1 above, the Fourier series expansion is given by [20].

$$V(wt) = \frac{4Vdc}{n\pi} \sum_{n=1,2,3,\ldots..}^{\infty} \{\cos(n\alpha_1) + \cos(n\alpha_2) + \ldots.. + \cos(n\alpha_s)\} \times \sin(nwt) \quad (3)$$

where α is the switching angle and *n= 1, 2, 3*…, Vdc is the DC supply voltage of the inverter and *S*is the number of switching angles.

Specifically, given a desired reference fundamental voltage V, there is need to find the switching angles, $\alpha_1, \alpha_2, \alpha_3, \ldots.. \alpha_s$, in such a way that, the total harmonic distortion of the voltage signal will be minimize.

From (3), the magnitude of the Fourier coefficients with respect to voltage *V* when normalized is as follows:

$$V = \frac{4Vdc}{\pi} \{\cos(\alpha_1) + \cos(\alpha_2) + \ldots.. + \cos(\alpha_s)\} \quad (4)$$

The amplitude of the fundamental component is controlled by the modulation index (*M*) and is given by the expression;

$$M = \frac{V}{Vdc} \quad (5)$$

where *V* is the maximum voltage output of the inverter.

The number of degrees of freedom for multilevel inverter using SHE technique equal to *S*; one of degrees of freedom is selected to find the value of *V*as presented in (6) and the remaining degree of freedom are selected to eliminate harmonic component. With this operation, higher order odd harmonic (*S*-1) will be eliminated [21]. By using (4) and (5), hence we can express the magnitude of the fundamental component as;

$$\cos(\alpha_1) + \cos(\alpha_2) + \cos(\alpha_3) + \ldots. + \cos(\alpha_{12}) = \frac{M\pi}{4} \quad (6)$$

while that of harmonic components are equated to zero.

The above non-linear transcendental equation is solved to find the approximate close value of the switching angles, capable of eliminating the inverter order harmonics at chosen modulation index. Due to the non-linearity of the equations, it is not possible to find the exact solution using ordinary mathematical methods, the numerical solution algorithm are presented in [7], [18] and [22].

In this research the analytical approach cited was not followed, due to some initial condition constrain and switching angle limitation which are also presented in [8]. Due to that, another approach was employed in order to obtain best switching angles with lowest THD as described in [10]. Half–Equal-Phase (HEP) method is used to arrange the main switching angles in a best possible way, it is used to obtain the output waveform wider and better, in the area between 0 to π/2 which are determine by the formula.

$$\alpha_i = i\frac{90^0}{\frac{m+1}{2}} = i\frac{180^0}{m+1} \quad (7)$$

where $i = 1, 2, \ldots, \frac{m-1}{2}$, and m is the inverter level.

Adjustment is made in (7) to extend the switching angle between *0* to *2π*, so that, all the possible switching angle combinations are accommodated, now *i= 0, 1, 2, 3 …24.*

III. Simulation Result

In order to validate the analytical result, the single phase 11-level cascaded H-bridge multilevel inverter has been simulated using PSIM software package platform. The switching angles of gating signal that control the twelve switches are obtained as desired and are presented in Fig. 5.

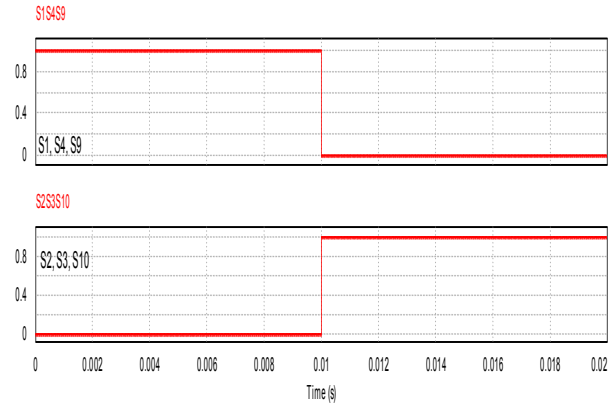

Fig. 5 (a) Switching signal of S_1, S_4, S_9 and S_2, S_3, S_{10}

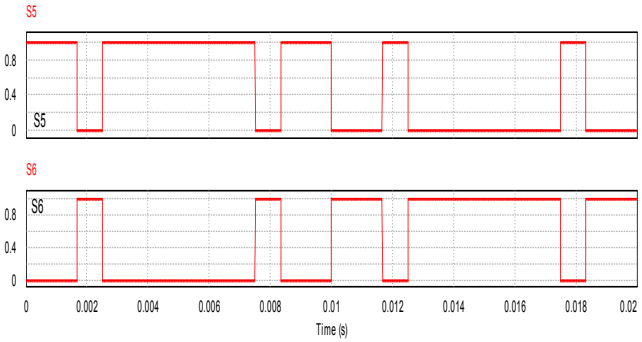

Fig. 5 (b) Switching signal of $S_5$and S_6

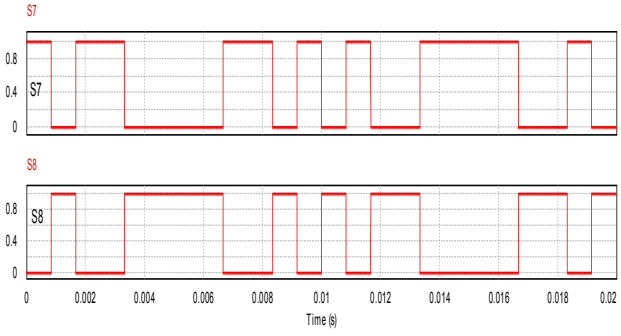

Fig. 5 (c) Switching signal of $S_7$and S_8

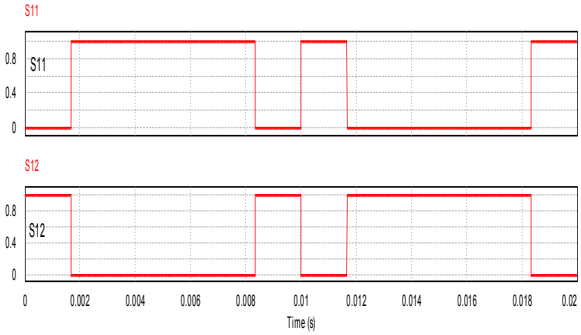

Fig. 5 (d) Switching signal of S_{11} and S_{12}

In any of the H-bridge modules, switches on the same leg are always operated complementary to avoid short circuiting the DC source. Total output voltage and harmonic analysis for the case study without isolation transformer is presented in Fig. 6 at fundamental frequency of 50 Hz.

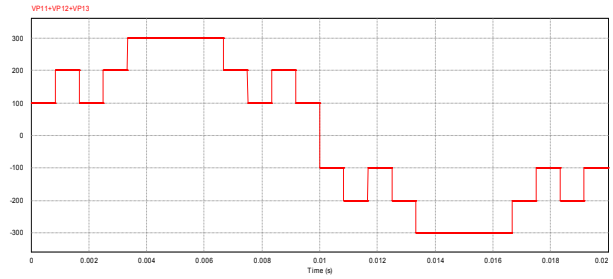

Fig. 6 (a) Voltage waveform of the inverter without isolation transformer at frequency of 50 Hz

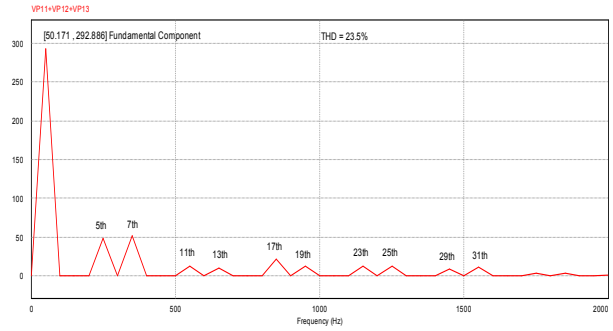

Fig. 6 (b) FFT analysis of the inverter without isolation transformer THD = 23.5%

Fig. 7 shows total output voltage analysis and harmonics contain for the case without isolation transformer at switching frequency of 5 KHz.

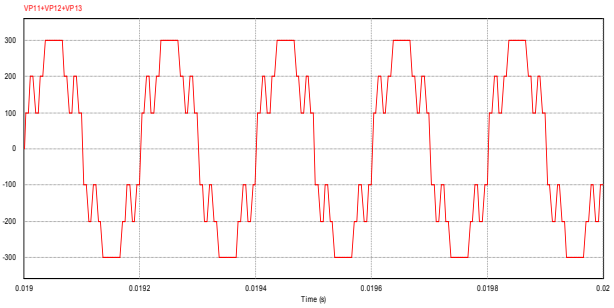

Fig. 7 (a) Voltage waveform of the inverter without isolation transformer at frequency of 5 KHz

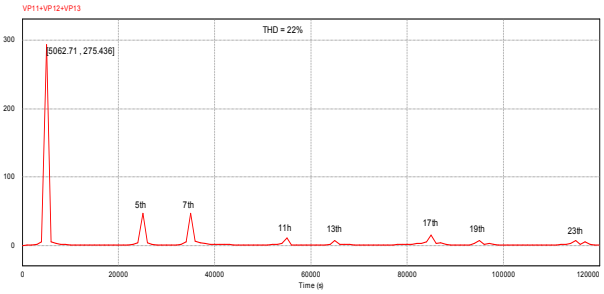

Fig. 7 (b) FFT analysis of the inverter without isolation transformer THD = 22%

Fig. 8 shows total output voltage analysis and harmonics contain for the case with isolation transformer at same frequency of 50 Hz.

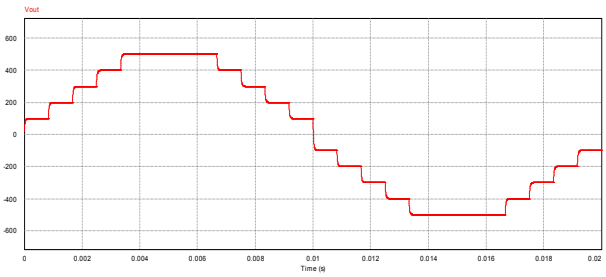

Fig. 8 (a) Voltage waveform of the inverter with isolation transformer at frequency of 50 Hz

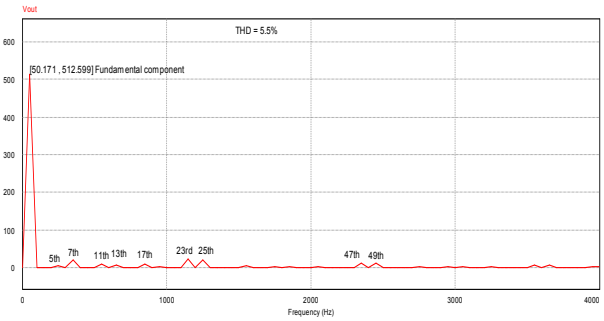

Fig. 8 (b) FFT analysis of the inverter with isolation transformer THD = 5.5%

Fig. 9 shows total output voltage analysis and harmonics contain for the case with isolation transformer at frequency 5 kHz.

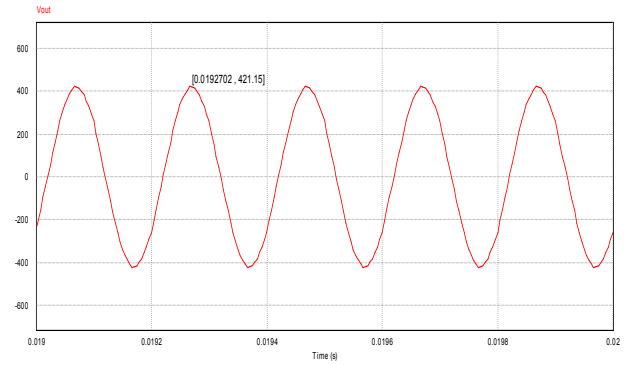

Fig. 9 (a) Voltage waveform of the inverter with isolation transformer at frequency of 5 KHz

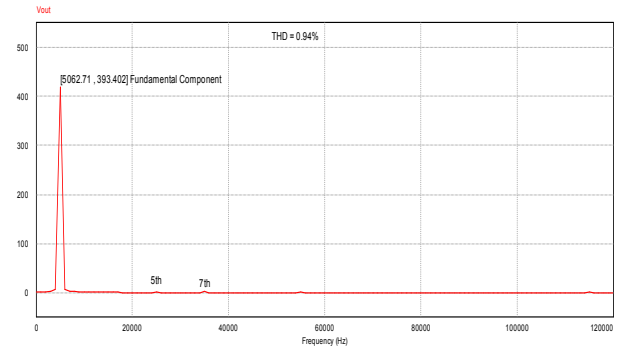

Fig. 9 (b) FFT analysis of the inverter with isolation transformer THD = 0.94%

From the FFT analysis result above, it can be seen that, there is tremendous reduction in THD from the two cases of 23.5% to 0.94%, this reduction arises because of the change in the inverter topology and switching frequency. In fact, switching at low frequency are required for high-power applications, so that switching losses are reduces to the minimum, and high switching frequency produces better power quality output and higher range of bandwidth, which are more preferable for high dynamic application ranges.

IV. Conclusion

An 11-level multilevel inverter using cascaded H-bridge topology with a single supply DC voltage source has been modelled and simulated. Two different cases have been investigated with two different frequencies, the first case without isolation transformer while the second case with isolation transformer. The second case produces more accurate results and both cases proved to be within the designed theories and results. The harmonic distortions contain available and magnitude level be contingent on the category of the inverter structure employed and modulation control used.

Based on the simulation results obtained for both cases, it appears SHE has the ability to eliminate selected harmonics by

chopping of the fundamental component at certain pre-determined angles. The inverter is able to eliminate eleven order odd harmonics, while the remaining higher frequency order harmonic will be eliminated with small size filter if desired. The higher triple harmonics are eliminated automatically due to proper configuration and symmetry of switching angle pattern arrangement. In addition, it satisfying the IEEE 5% THD within the targeted range, IEEE STD 519 – 1992 harmonic limit.

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