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Design and Analysis of an 8T Read Decoupled Dual Port SRAM Cell for Low Power High Speed Applications

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***Abstract*—**Speed, power consumption and area, are some of the most important factors of concern in modern day memory design. As we move towards Deep Sub-Micron Technologies, the problems of leakage current, noise and cell stability due to physical parameter variation becomes more pronounced. In this paper we have designed an 8T Read Decoupled Dual Port SRAM Cell with Dual Threshold Voltage and characterized it in terms of read and write delay, read and write noise margins, Data Retention Voltage and Leakage Current. Read Decoupling improves the Read Noise Margin and static power dissipation is reduced by using Dual-V_t transistors. The results obtained are compared with existing 6T, 8T, 9T SRAM Cells, which shows the superiority of the proposed design. The Cell is designed and simulated in TSPICE using 90nm CMOS process.

***Keywords*—**CMOS, Dual-Port, Data Retention Voltage, 8T SRAM, Leakage Current, Noise Margin, Loop-cutting, Single-ended.

I. Introduction

WITH scaling of devices to the nanometer regime, the problems of static power dissipation, cell stability due to variation in process parameters and noise in memory cells become a matter of concern. Considerable amount of power is consumed during memory accesses, which greatly reduces battery life in portable applications like mobile phones and PDAs. Hence efficient SRAM designs are required to address the active and leakage power consumption problems in low power applications. The data read operation of SRAM cells must be non-destructive and static noise margin must be in acceptable range. The bit yield of SRAM cells depends on several factors such as supply voltage, threshold voltage and transistor-sizing ratios. The lowest operational voltages of SRAM cells are limited by the cell stability and write ability. The area of the SRAM Cell is also very important as it contributes to the silicon area and power consumption.

In this paper, the first section discusses the existing SRAM Cells- 6T, 8T and 9T, and their limitations. Our design is proposed in this section. Minimum-sized transistors are used in our design to achieve minimum silicon area. High and low threshold voltage (V_t) transistors are used in the cell.The cell and pull-up ratios are optimized to active high speed and improved noise margin. In the second section of the paper, the simulation results using TSPICE in 90nm CMOS process, is discussed and compared with the previous SRAM cells.

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II. SRAM Cell

The conventional 6T SRAM cell suffers from the problem of destructive read and has reduced noise margin. The data storage nodes are accessed directly through the pass transistors by the bit-lines. Interference of the bit-line voltage with the internal nodes of the cell reduces the noise margin of the cell. Proper transistor sizing in terms of cell ratio and pull-up ratio is required to optimize the noise margin of the cell. For cell stability during read operation, storage inverters are usually made strong and the pass-gates weak. Conversely, for write ability, weak storage inverters and strong pass-gates are favorable.

The 8T and 9T SRAM cells both employ the read-decoupling mechanism, isolating the bit-line from the storage nodes of the cell, hence considerably improving the read noise margin [5]. However, the 8T SRAM cell has lower write margin due to absence of complementary bit-line. Moreover, the leakage current in the 8T SRAM cell during HOLD mode is more. Also having a single port for both read and write operation, the cell can be accessed at one address at a time, thus, read/write operations can be performed in only one memory cell at each clock cycle. The 9T SRAM Cell occupies larger cell area. However, the power consumption is reduced by using Dual-V_t transistors. Read delay is increased slightly due to use of high threshold voltage transistors.

A. Proposed 8T SRAM Cell

The proposed Dual-port 8T SRAM cell employs read decoupling with read and write assist transistors. Sizing of the read and write assist transistors are crucial for efficient performance of the cell. Overestimating the size of transistors leads to loss in silicon area and increased power consumption, while underestimating the size leads to increased resistance and delays [6].

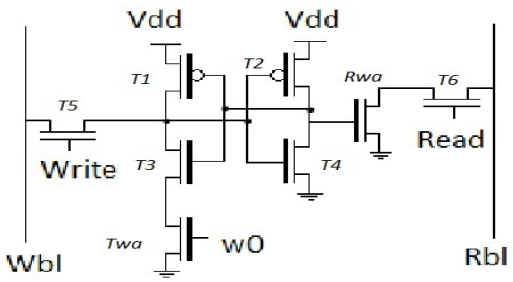

Fig. 1 Structure of proposed 8T SRAM Cell. Dark transistors indicate high-V_t and light transistors indicate low-V_t.

The structure of the proposed SRAM Cell is shown in Fig. 1. The read and write assist transistors are denoted as 'R_{wa}' and 'T_{wa}' respectively. The cross-coupled inverters, read and write assist transistors have a high threshold voltage and the access transistors have a low threshold voltage. The high threshold voltage transistors reduce leakage current of the cell in standby mode, hence limiting static power dissipation. The access transistors have a low threshold voltage to ensure minimum read and write delays and high speed operation.

TABLE I
THRESHOLD VOLTAGE OF NOMINAL AND HIGH V_t NMOS/PMOS

	Nominal V_t	High V_t
PMOS	-0.139V	-0.4V
NMOS	0.169V	0.448V

TABLE II
TRANSISTOR SIZES USED IN THE PROPOSED DESIGN

TRANSISTOR	WIDTH (nm)
T_{wa}, R_{wa}	12
T1,T2,T3,T4	20
T5	100
T6	200

Minimum-sized transistor is used for write for write assist so as to form a high resistance path to ground, which would effectively break the feedback loop during write operation. The Cell Ratio and Pull-up Ratio of our design are 0.1 and 0.2 respectively. The transistor sizes used in our design is given in Table II.

B. Read Operation

The R_{bl} is pre-charged to V_{dd} before every read operation and W_0 is kept '1' to sustain the latch operation. When Q is '0' and Q_B is '1' (cell storing a '0') and Read is '1', R_{wa} is ON and forms a discharge path for the read bit-line to ground, which gives a successful read operation. Again, when Q is '1' and Q_B is '0' (cell storing '1') and Read is '1', R_{wa} is OFF and the read bit-line voltage is maintained at V_{dd} . The threshold voltage of R_{wa} is kept high to ensure that there is minimum leakage current during a read '1' operation and the voltage in R_{BL} is maintained at V_{dd}.

C. Write Operation

During every write operation W_0 is made '0'. This turns T_{wa} OFF, weakening the feedback loop to ensure a successful write operation. WRITE is '1' during write operation. Initially, when Q is '0' and Q_B is '1' (cell storing '0') and we want to write a '1', it is difficult to force the node Q to '1' through a pass transistor as the inverters are strongly cross-coupled. Hence the pull-down strength of the first inverter has to be weakened through the series transistor T_{wa}[6]. When a '0' has to be written to a cell initially storing a '1' the node Q discharges through T5 and W_{bl}, thus making a successful write operation.

During HOLD state, W_0 is kept high for normal operation of the latch and READ and WRITE signals are kept low.

III. EXPERIMENTAL RESULTS

The proposed 8T SRAM cell is characterized in terms of Read Noise Margin (RNM), Write Noise Margin (WNM), Read Delay, Write Delay, Data Retention Voltage (DRV) and Power Dissipation. The results are compared with the existing SRAM cells [1], which show our design to have better performance. The comparisons are done at a supply voltage of 1.2V.

A. Read Noise Margin

The read noise margin is improved through isolation of the read current path from storage node Q_b[7].

TABLE III
READ NOISE MARGIN OF DIFFERENT SRAM CELLS

SRAM CELL	RNM (V)
6T	0.084
8T	0.314
9T	0.299
This work	0.31

From Table III, we can see that the read noise margin of the proposed design is 269% and 3.67% higher than the conventional 6T cell and 9T cell respectively.

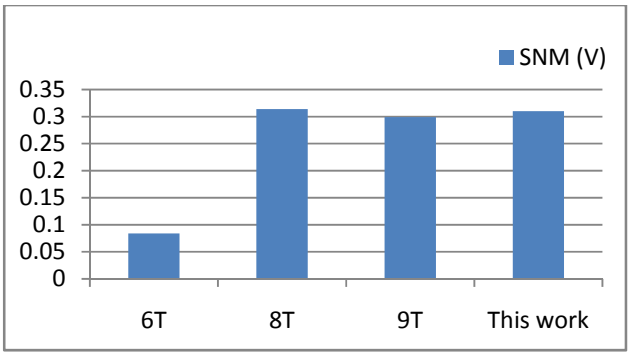

Fig. 2 Read Noise Margin in different SRAM Cells

The Read Noise Margin is analyzed using the butterfly curve obtained from the cross-coupled inverters as shown in Fig. 3. The Noise Margin is given as the side of the largest square which can be drawn between the inverter characteristics [4]. Decoupling read port avoids read disturb issue for the activated word-line. This makes the noise margin during HOLD state same as the Read Noise Margin.

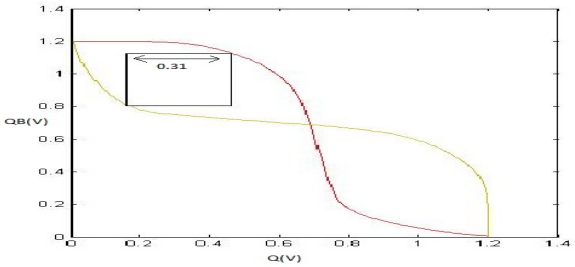

Fig. 3 Butterfly Curve for Read Noise Margin. The side of the maximum sized square indicated the noise margin as 0.31V

B. Write Noise Margin

The write noise margin is calculated using the bit-line sweeping method. It is characterized by the write trip voltage which is defined as the maximum bit-line voltage required to flip the cell content.

TABLE IV
WRITE NOISE MARGIN OF DIFFERENT SRAM CELLS

SRAM CELL	WNM (V)
6T	0.479
8T	0.445
9T	0.757
This work	0.613

From Table IV, we can see that the write noise margin of the proposed design is 27.9% and 37.7% higher than the 6T cell and 8T cell respectively.

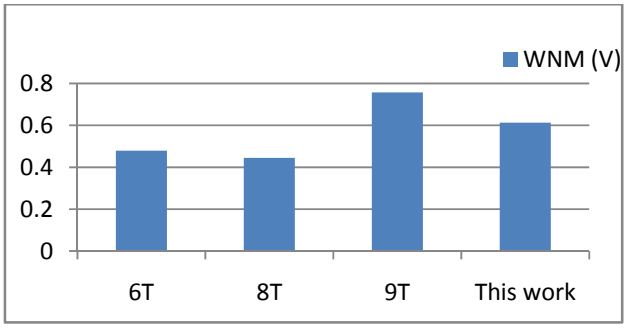

Fig. 4 Write Noise Margin in different SRAM Cells

Fig. 5 shows the trip off voltage of the SRAM Cell. The writ bit-line is swept from 0 to 1.2V which shows us that the cell flips its state at 0.613V.

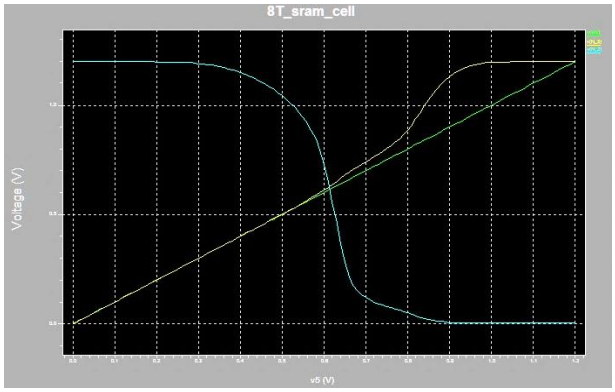

Fig. 5 Bit-Line voltage sweep at node Q indicating the trip-off voltage of the SRAM Cell

C. Read Delay

TABLE V
READ DELAY OF DIFFERENT SRAM CELLS

SRAM CELL	READ DELAY (ps)
6T	72.82
8T	77.72
9T	98.85
This work	15.93

The read delay of the proposed design is much faster the existing SRAM cells. This is due to isolation of the read port from the storage node of the cell.

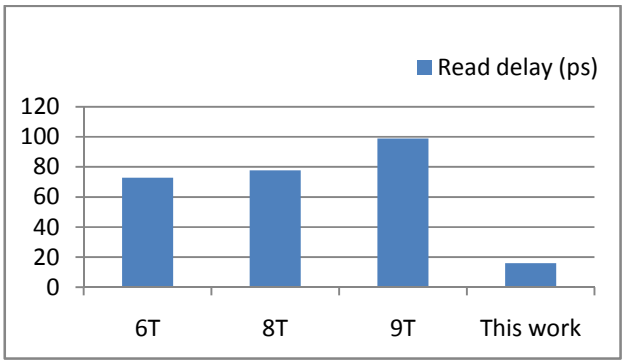

Fig. 6 Read Delay in different SRAM Cells

D. Write Delay

The write delay of the proposed SRAM Cell is sufficiently improved over the existing 6T and 8T SRAM cells. Employing the write assist transistor helps in cutting the feedback loop of the cross-coupled inverters and hence ensures a faster write operation.

TABLE VI
WRITE DELAY OF DIFFERENT SRAM CELLS

SRAM CELL	WRITE DELAY (ps)
6T	8.976
8T	45.47
9T	10
This work	8.90

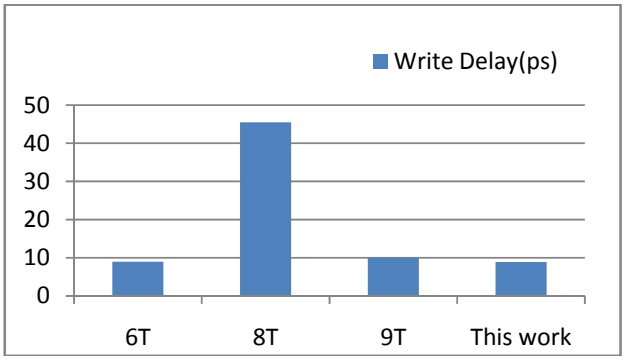

Fig. 7 Write Delay in different SRAM Cells

From Fig. 7, we can see that the proposed 8T SRAM cell is 80.42% faster than the existing 8T cell, which does not have a complementary bit line to aid during the write operation and hence the storage node cannot discharge fast. This also makes the cell more prone to noise.

E. Data Retention Voltage (DRV)

The noise margin of the cell decreases with decrease in supply voltage V_{dd}. The minimum supply voltage which is supported by the cell beyond which the cell state flips is the Data Retention Voltage [1].

TABLE VII
DATA RETENTION VOLTAGE OF DIFFERENT SRAM CELLS

SRAM CELL	DRV (mV)
6T	252.2
8T	93.64
9T	84.5
This work	300

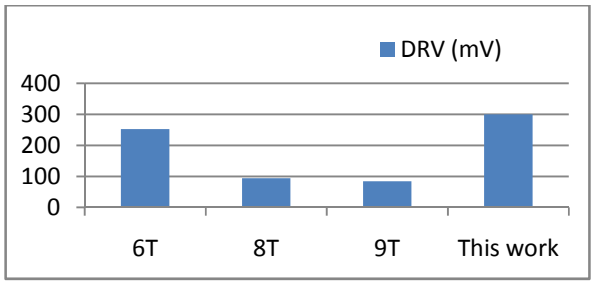

Fig. 8 Data Retention Voltage of different SRAM Cells

From Fig. 8, we can see that the data retention voltage of the proposed design is degraded from the existing SRAM cells. This is primarily due to use of high threshold voltage transistors in the cell, which reduces the current in the cell required to sustain the latch operation during standby mode.

F. Power Consumption

The average write power consumption of the proposed design is compared with the 6T, 8T and 9T SRAM Cells.

TABLE VIII
WRITE POWER CONSUMPTION OF DIFFERENT SRAM CELLS

SRAM CELL	Write Power Consumption (uW)
6T	0.32
8T	1.88
9T	2.02
This work	1.71

Table VIII shows us that the write power consumption of the proposed cell is higher than the 6T cell due to increase in number of transistors.

TABLE IX
STATIC POWER CONSUMPTION OF PROPOSED CELL WHILE STORING '0' AND '1' RESPECTIVELY

	While storing '0' (uW)	While storing '1' (uW)
Static Power Consumption	0.212	0.445

However, the static power consumption of our design during the HOLD state is reduced by 18.7% using dual-V_t transistors over the single-V_t transistors, which limits the sub-threshold current in the cell [2], [3]. While storing '1', the transistors T2 and T3 conduct leakage current which passes to ground via the extra active write-assist transistor T_{wa}. However, while storing '0', only the transistors T1 and T4 conduct leakage current to ground. Hence, the static power consumption while storing '0' is less than while storing '1'.

IV. CONCLUSION

This paper discusses a read-decoupled dual-port 8T SRAM cell based on dual-V_t transistors using 90nm CMOS process. It achieves a Read and Write Noise Margin of 0.31V and 0.613V respectively at a supply voltage of 1.2V. It has a Read and Write Delay of 15.93ps and 8.90ps respectively, making it ideal for high speed applications. The static power dissipation during HOLD state is reduced using dual-V_t transistors, making it suitable for low power applications. The cell also occupies lesser silicon area than the existing 9T SRAM Cell.

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