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A Current Steering Positive Feedback Improved Recycling Folded Cascode OTA

S. Kumaravel, B. Venkataramani

***Abstract*—**In the literature, Improved Recycling Folded Cascode (IRFC) Operational Transconductance Amplifier (OTA) is proposed for enhancing the DC gain and the Unity Gain Bandwidth (UGB) of the Recycling Folded Cascode (RFC) OTA. In this paper, an enhanced IRFC (EIRFC) OTA which uses positive feedback at the cascode node is proposed for enhancing the differential mode (DM) gain without changing the unity gain bandwidth (UGB) and lowering the Common mode (CM) gain. For the purpose of comparison, IRFC and EIRFC OTAs are implemented using UMC 90nm CMOS technology and studied through simulation. From the simulation, it is found that the DM gain and CM gain of EIRFC OTA is higher by 6dB and lower by 38dB respectively, compared to that of IRFC OTA for the same power and area. The slew rate of EIRFC OTA is also higher by a factor of 1.5.

***Keywords*—**Cascode Amplifier, CMRR, g_m/I_D Methodology, Recycling, Slew Rate.

I. Introduction

HIGH performance Analog to Digital Converters (ADC) and switched capacitor (SC) filters require Operational Transconductance Amplifiers (OTAs) that has both high DC gain and a high unity gain bandwidth (UGB). The advent of deep sub-micron technologies enables increasingly high speed circuits. As the technology scales down, the intrinsic gain $g_m r_o$ of the transistor decreases which makes it difficult to design OTAs with high DC gain. In low voltage CMOS process, Folded Cascode (FC) amplifier is one of the most preferred architectures for both single stage and for the first stage of the multi-stage amplifiers due to its high gain and reasonably large output signal swing. Moreover, the FC with PMOS input pair is preferred over its NMOS counterpart due to its higher non-dominant poles and lower flicker noise [1], [2].

A number of techniques have been proposed in the literature to enhance the gain of the FC OTA. One of these techniques presented in [3], [4] enhances the DC gain by providing an additional current path at the cascode node. This converts the current source into active current mirror which raises the output current to be above its quiescent value during slewing. Another technique proposed in [5], enhances the DC gain and UGB by modifying the bias current sources of the FC OTA. These current sources do not contribute to DC gain. A recycling technique is proposed to overcome this disadvantage. This OTA is referred to as Recycling Folded Cascode (RFC).

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In [6], further enhancement in the DC gain and UGB of the RFC OTA is obtained using Improved Recycling structure and is termed as IRFC OTA. In this paper, an enhanced IRFC (EIRFC) OTA is proposed, by adopting the technique proposed in [3], [4] for the FC OTA. The performance of the two OTAs (IRFC and EIRFC) are evaluated through simulation and compared.

The paper is organized as follows. Section II presents an overview of the IRFC OTA. Section III gives an overview of the problem at the cascode node. Section IV describes about the enhanced IRFC OTA proposed in this paper. Sections V and VI present the simulation results and the conclusion respectively.

II. Improved Recycling Folded Cascode OTA Overview

The folded cascode OTA [1] is shown in Fig. 1. In this OTA, the bias current sources M3 and M4 draw high current, and have large transconductance. However, these current sources do not contribute to the DC gain. In order to ensure that M3 and M4 also contribute to the DC gain, the RFC OTA is proposed in [5] and is shown in Fig. 2. In this OTA, the input transistors of FC are split into two parts (M1a, M1b, M2a, M2b) which conduct fixed and equal currents of $I_b/2$. Bias transistors M3 and M4 are split into two parts M3a, M3b and M4a, M4b respectively in the ratio of K:1 where the value of K may chosen to be 2 to 4. The transistors M2b, M11, M3b form a unity gain configuration such that the input signal V_{in}- fed to M2b has the same phase and magnitude at the input of M3a and M3b as that of V_{in}+ fed to M1a. Transistors M11 and M12 are added for improved matching of current between M3a and M3b. Similarly, M1b, M12, and M4b form a unity gain configuration. To improve the signal swing at the current mirror nodes X+ and X-, the DC and AC path are separated in IRFC proposed in [6] and is shown in Fig. 3. To achieve this, the transistors M11, M3b and M12, M4b are divided into two parts M11a, M11b, M3b1, M3b2 and M12a, M12b, M4b1, M4b2 respectively. The paths M11b, M3b2 and M12b, M4b2 have high impedance ($g_{m11b} r_{011b} r_{03b2}$). The paths M11a, M3b1 and M12a, M4b1 and have low impedance ($1/g_{m3b1}$). The small signal current flows through the low impedance path. The ratio of DC currents flowing through the high impedance and low impedance paths is a:b and the transconductance of M11a, M3b1 is scaled by 'a' where a < 1. The signal flowing through the current mirror node becomes larger compared to that of the RFC due to the increase in the resistance of the small signal path.

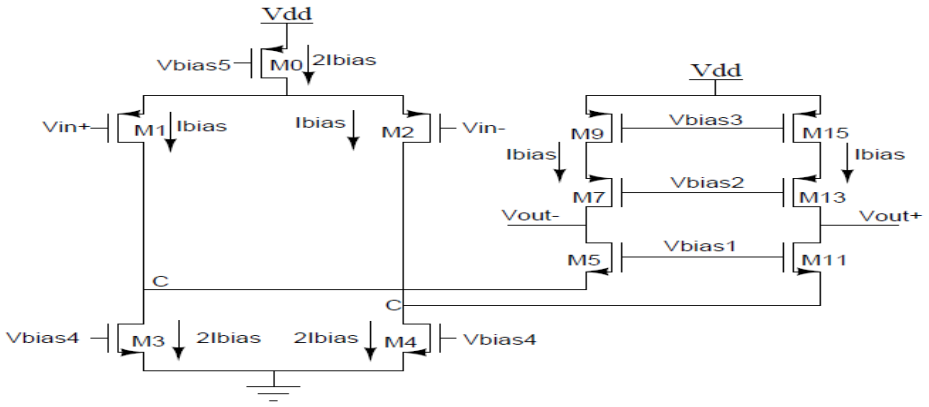

Fig. 1 Folded Cascode OTA

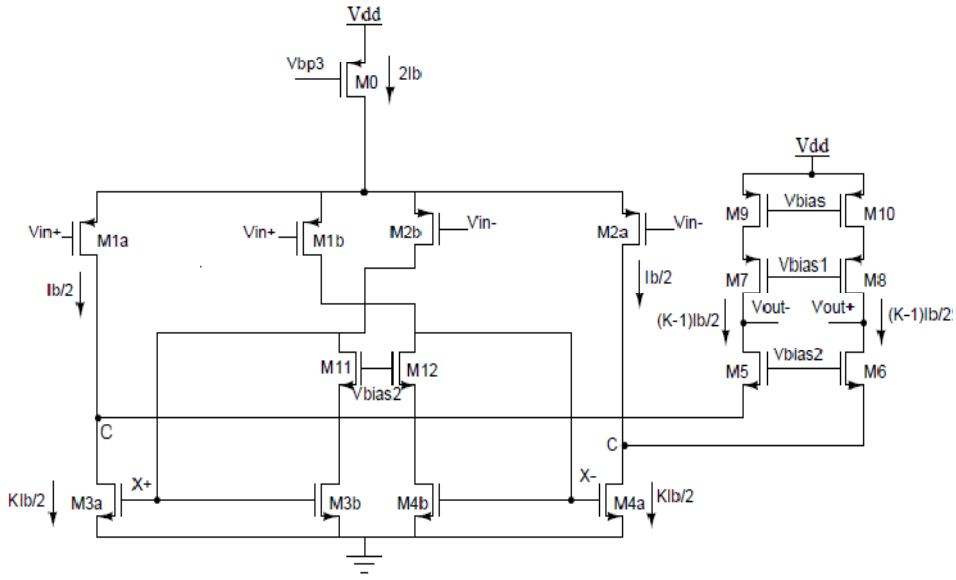

Fig. 2 Recycling Folded cascode OTA

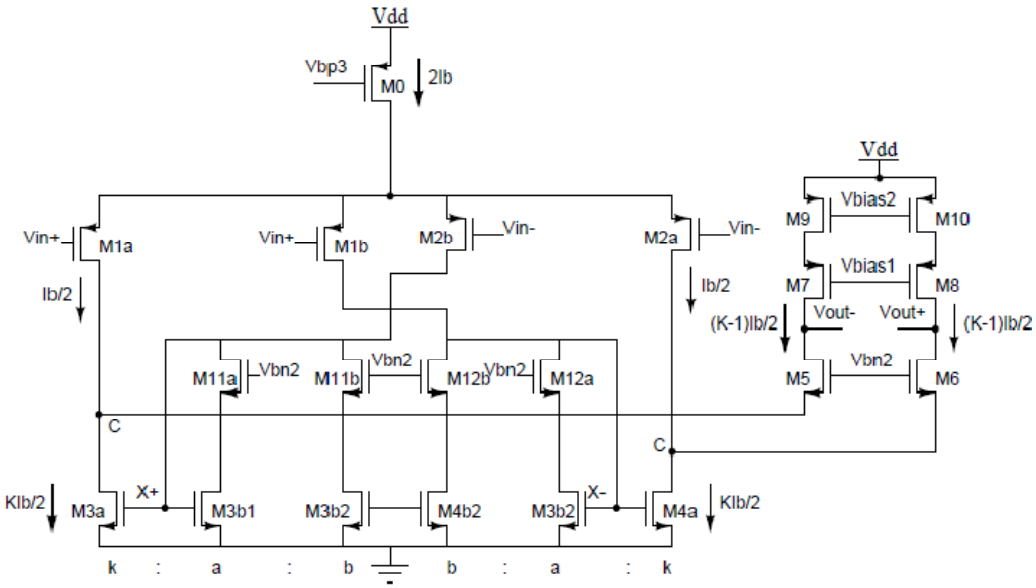

Fig. 3 Improved Recycling Folded Cascode OTA

A. DC Gain

The DC gain A_v of the OTA is given by (1)

$$A_v = G_m * R_{out} \quad (1)$$

where G_m is the transconductance and R_{out} is the output impedance. $G_{m,IRFC}$, the transconductance of IRFC OTA is given by

$$G_{m,IRFC} = I_{out}/V_{in+} \quad (2)$$

where the output current I_{out} is given by

$$I_{out} \approx g_{m1a}V_{in+} + g_{m3a}V_{x+} \quad (3)$$

From Fig. 3, it can be seen that transistors M2b and the diode connected transistors M11a and M3b1 act as a common source amplifier with a voltage gain of approximately $-1/a$. Since, the input applied to M2b is in opposite direction, the voltage at node X_+ (or X_-) has the same phase as that of V_{in+} (or V_{in-}) where

$$V_{x+} \approx -g_{m2b}R_xV_{in-}$$

$$R_x = 1/a.g_{m3b1}$$

Hence

$$V_{x+} \approx \frac{-V_{in-}}{a}$$

Substituting V_{x+} in (3)

$$I_{out} = g_{m1a}V_{in+} + \frac{1}{a}g_{m3a}V_{in+} \quad (4)$$

Substituting (4) in (2) gives the small signal transconductance G_m.

$$G_{m,IRFC} = g_{m1a} + \frac{1}{a}.g_{m3a} \quad (5)$$

where

$$g_{m3a} \approx K.g_{m1a}$$

The output impedance $R_{out,IRFC}$ of the IRFC OTA is given by

$$R_{out,IRFC} = g_{m5}r_{05}(r_{01a}||r_{03a})||g_{m7}r_{07}r_{09} \quad (6)$$

Substituting (5) and (6) in (1) the A_v of IRFC OTA is given by (7)

$$A_v = g_{m1a}(\frac{K}{a} + 1) * g_{m5}r_{05}(r_{01a}||r_{03a})||g_{m7}r_{07}r_{09} \quad (7)$$

B. Frequency Response Analysis

From Fig. 3, it is observed that there are three poles and one zero. The expressions for the three poles are given below.

1. Dominant Pole

Because of high impedance ($R_{out,IRFC}$) and large capacitance (C_{out}) at the output node, the dominant pole occurs in this node. The dominant pole frequency ω_{p1} (f_{-3db}) is given by

$$\omega_{p1} = 1/R_{out,IRFC}C_{out} \quad (8)$$

where

$$R_{out,IRFC} \approx g_{m5}r_{o5}(r_{01a}||r_{03a})||g_{m7}r_{07}r_{09}$$

and

$$C_{out} = C_l + C_{DB8} + C_{GD8} + C_{GD6} + C_{DB6}$$

2. Non-Dominant Pole-1

It occurs in the cascode node C at a higher frequency compared to the dominant pole. Since the output capacitance bypasses the effect of output impedance, an equivalent impedance R_C at the cascode node is approximately equal to $1/g_{m5}$. Hence, the non-dominant pole frequency ω_{p2} is given by

$$\omega_{p2} = 1/R_CC_C \quad (9)$$

where

$$C_C \approx C_{GD3a} + C_{GS5} + C_{GD1a} + C_{DB3a} + C_{DB1a} + C_{SB5}$$

3. Non-Dominant Pole-2

The second non dominant pole ω_{p3} is at the current mirror node X_+ or (X_-) and is determined by the node capacitances at that node (C_x) and impedance seen at that node (R_x) at higher frequencies, which are given as follows

$$\omega_{p3} = 1/R_XC_{Xx} \quad (10)$$

where

$$R_X = \frac{1}{g_{m3b1}}$$

$$C_X = C_{GD3A} + C_{GS5} + C_{GD1a} + C_{DB3a} + C_{DB1a} + C_{GS3b1} + C_{GD3b1} + C_{GD11a} + C_{BD11a} + C_{GD11b} + C_{DB11b} + C_{GD2b} + C_{DB2b}$$

The UGB of the OTA is given by

$$UGB = A_v * f_{-3dB} \quad (11)$$

Substituting (7) & (8) in (11)

$$UGB \approx g_{m1a}(\frac{K}{a} + 1)/C_L \quad (12)$$

From (7) & (12), it is observed that the A_v and UGB are enhanced by a factor of $1/a$, compared to the RFC OTA [5] for the same power and area.

III. Current Steering Positive Feedback

In Fig. 4, the drain current ($i_{ds} = g_m v_{in}$) of the input transistor M1 flows through two paths at the cascode node C. One path is formed by r_{o1} of the input transistor M1 and the

other path is formed by the impedance (Z_C) looking into the source of cascode transistor M2. The input impedance of the Common Gate (CG) amplifier is given by,

$$Z_C = \frac{1}{g_{m2}}\left(1 + \frac{R_{load}}{r_{02}}\right) \quad (13)$$

Z_c can be analyzed for two cases.

A. Case 1:

If the load impedance (R_{load}) of M2 is realized using a cascode current source, it can be shown [1] that Z_C is given by

$$Z_C = \frac{1}{g_{m2}}\left(1 + \frac{R_{load}}{r_{02}}\right) \cong \frac{R_{load}}{g_{m2}r_{02}} = \frac{g_{m3}r_{03}r_{04}}{g_{m2}r_{02}} \cong r_{04} \quad (14)$$

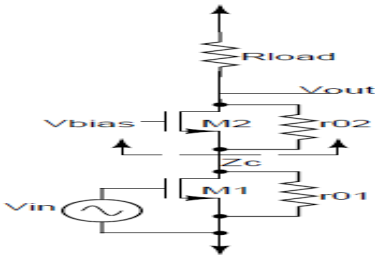

Fig. 4 Cascode amplifier

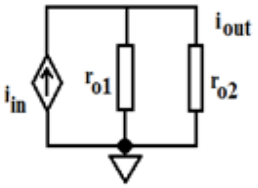

Fig. 5 Common Gate amplifier when R_{load} is cascode load.

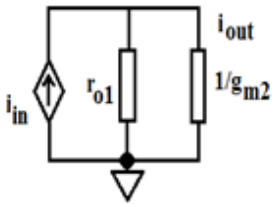

Fig. 6 Common Gate amplifier when R_{load} << ro2.

From (14), it can be noted that Z_C is almost equal to the output impedance. As a result $i_{in}(i_{ds})$ is distributed almost equally through r_{o1} and Z_C . From Fig. 5, the current gain ∝, is halved, hence the common gate amplifier cannot be treated as buffer. The current flowing through Z_C generates V_{OUT}. The empirically observed DC gain (V_{OUT}/V_{in}) of the cascode amplifier is typically less than the theoretical value $(g_m r_0)^2$ [3].

B. Case 2:

If the load impedance (R_{load}) of M2 is << ro2, it can be shown that Z_C is given by $1/g_{m2}$. From Fig. 6, the current gain ∝, is unity.

$$Z_C = \frac{1}{g_{m2}}\left(1 + \frac{R_{load}}{r_{02}}\right) \cong \frac{1}{g_{m2}} \quad (15)$$

For this case, the advantage of using cascode impedance in cascode amplifiers is nullified. So the cascode amplifiers DC gain will be degraded.

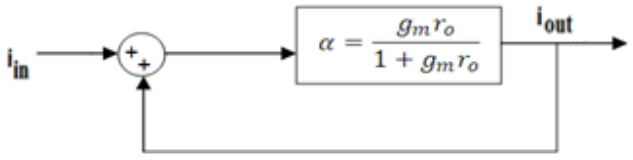

Fig. 7 Positive feedback technique

In order to increase the DC gain, the current flowing through Z_C should be increased. This can be achieved by incorporating a current-based positive feedback technique at the cascode node C shown in Fig. 7, where the current gain is amplified by the factor of 2 and $g_m r_o$ respectively for both cases. This technique is proposed for the fully differential FC OTA in [3]. The FC OTA incorporating this method is referred to as Enhanced FC OTA [4]. In Fig. 8, the positive feedback configuration is shown for FC OTA. This method is adopted for IRFC OTA in this paper.

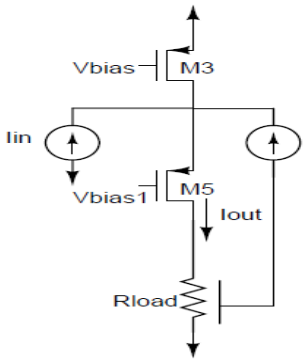

Fig. 8 Positive feedback for folded Cascode Amplifier

IV. Enhanced FC OTA

The input impedance Z_C at the cascode node C of the FC OTA shown in Fig. 3, is given by (16)

$$Z_C \approx \frac{1}{g_{m5}}\left(1 + \frac{g_{m7}r_{07}r_{09}}{r_{05}}\right) \quad (16)$$

$$\cong \frac{g_{m7}r_{07}r_{09}}{g_{m5}r_{05}}$$

In [4], the cascode node of the FC OTA is modified and the current sources are replaced with an active inverting current mirror. The same approach is adopted for the IRFC OTA at the cascode node. The modified half circuit of IRFC OTA is shown in Fig. 10. The active load of the IRFC OTA comprising (M7, M9) is modified into an active inverting current mirror comprising (M7, M9, M15, M17, and the inverters). A normal current mirror creates a copy of a current of equal magnitude and in the same direction. The inverting current mirror creates a copy of any incremental currents that is equal in magnitude, but opposite in direction. The inverting

incremental currents for M7 and M9 can be obtained from M2a and hence the inverters shown in Fig. 10 are not required. Therefore, M13, M15 and M17 are attached to the drain of M2a. The fully differential enhanced IRFC OTA is shown in Fig. 9. The expressions for the gain from the cascode node to the output node and the modified input impedance Z_C at the cascode node [4] are given by (17) & (18),

$$\frac{v_{out}}{v_C} \cong (g_{m5} + g_{m14}) r_{o5} \quad (17)$$

$$Z_C \cong \frac{g_{m7} r_{07} r_{09}}{2 g_{m5} r_{05}} \quad (18)$$

Comparing (16) and (18), it can be concluded that Z_C is reduced by a factor of 2.

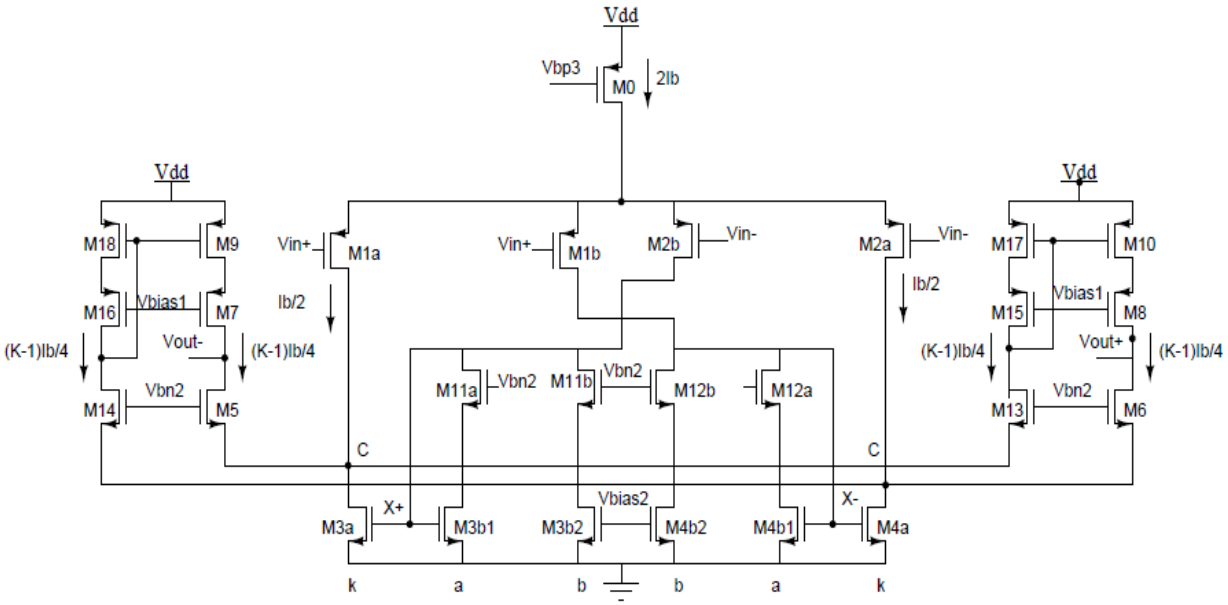

Fig. 9 Proposed Enhanced IRFC OTA

A. Description of EIRFC

Next, the operation of the fully differential EIRFC is described. In the half circuit shown in Fig. 10 of the EIRFC, an input voltage of Vin_+ is applied to the M1a and Vin- is applied to the M2b. M2b acts as a common source amplifier with a diode connected load whose impedance looking into the drain of M11a is given by $1/a.g_{m3b1}$. M11b and M3b2 provide a very high impedance path and hence all the current flows through M11a and M3b1. The output voltage of M2b is given to the gate of M3b1 and M3a which is used for the current mirror action. It copies K/a times of the current in M3b1 to M3a. Both the inputs at M1a and M3a are in phase. The current produced by M1a and M3a is now given to the cascode node C. At the cascode node, i.e. at the drain of the M1a and M3a, the current sees multiple current paths formed by the cascode transistors M5 and M13. The impedance looking into the source of M5 is of the order of output impedances exhibited by transistor M7 and M9 which is equal to $g_{m7} r_{07} r_{09}$. The impedance looking into the source of M13 has two diode connected transistors M15 and M17 in series as a load whose impedance is approximately equal to $1/g_{m15}$. Therefore, the path into M13 has significantly lower impedance compared to the other competing paths attached to the cascode node C. Hence, a major fraction of the input current flows into the source of M13 at low frequencies. By the current mirror action of M15, M17, M8 and M10, nearly all the input current is effectively mirrored onto the non-inverting output of the amplifier.

In order to carry out positive current feedback, the current at the non-inverting output is fed directly back to the input section (without inversion). The current at the non-inverting output flows into the other cascode node through transistor M6. The impedance looking into the source of M14 is negligible compared to the impedance as exhibited by other competing current paths at this cascode node. Hence, majority of the current flows into the source of M14.

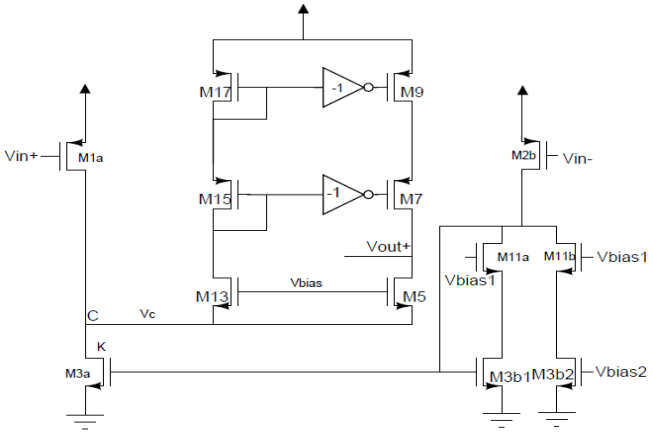

Fig. 10 Half circuit of EIRFC

By the current mirror action of M16, M18, M7 and M9, source current of M6 is effectively mirrored onto the inverting output. The resulting current at the inverting output flows back into the original cascode node through M5. Similar operation occurs in the other half of the signal at the gate of M2a. Thus the current at the non inverting node is effectively fed back to the starting node. This positive feedback operation gives a higher output resistance (19) and hence a higher gain (21). If g_{m5} and g_{m13} are equal, then the output resistance increases by two times and the gain of the EIRFC amplifier is also increased by two times as compared to the IRFC.

B. DC Gain

$$R_{out,EIRFC} \approx (g_{m5} + g_{m13)} r_{05}(r_{01a} || r_{03a}) || g_{m7} r_{07} r_{09} \quad (19)$$

$$G_{m,EIRFC} \approx g_{m1a}\left(1 + \frac{K}{a}\right) \quad (20)$$

The A_v of the EIRFC OTA is calculated using (19) and (20) in (1), and is given by (21)

$$A_v \approx g_{m1a}\left(\frac{K}{a} + 1\right) * \{(g_{m5} + g_{m13}) r_{05}(r_{01a} || r_{03a}) || g_{m7} r_{07} r_{09}\} \quad (21)$$

From (21), it is observed that A_v of EIRFC OTA is 2 times higher than that of IRFC OTA.

C. Frequency Response

The proposed op amp has three poles: the dominant pole at the output node and the non dominant poles at the cascode node (at the drain node of the input transistor (M1, M2) and a pole at current mirror node X+(or X-). Frequency response of the op amp can be analyzed using the differential half-circuit shown in Fig. 10.

1. Dominant Pole:

Because of high impedance (R_{out}) and large capacitance (C_{out}) at the output node, the dominant pole occurs in this node.

The dominant pole frequency ω_{p1} is given by

$$\omega_{p1} = 1/R_{out,EIRFC} C_{out} \quad (22)$$

where

$$R_{out,EIRFC} = (g_{m5} + g_{m11)} r_{05}(r_{01a} || r_{03a}) || g_{m7} r_{07} r_{09}$$

and C_{out} denotes the equivalent load capacitance, which includes the external capacitance C_L and all the parasitic junction capacitances associated with the output node.

$$C_{out} \approx C_L + C_{DB8} + C_{GD8} + C_{GD12} + C_{DB12}$$

2. Non-Dominant Pole-1:

The non-dominant pole is determined by the intrinsic capacitances existing at the cascode node C and the effective cascode input impedance R_C at high frequencies. Although the impedance at the cascode node for DC is high, at low frequencies, the drain of M5 is short circuited to ground by C_L beyond the dominant pole frequency. Hence, the impedance at the source of both M5 and M8 is approximately equal to $1/g_{m5}$. Hence, the non-dominant pole ω_{p2} is given by

$$\omega_{p2} = 1/R_C C_C \quad (23)$$

where

$$R_C = 1/2g_{m5}$$

and

$$C_C = C_{GD3A} + C_{GS5} + C_{GD1a} + C_{DB3a} + C_{DB1a} + C_{SB5}$$

3. Non-Dominant Pole-2:

The second non dominant pole is at the current mirror node X and is determined by the node capacitances at that node (C_X) and impedance seen at that node (R_X) at higher frequencies, which are given as follows

$$\omega_{p3} = 1/R_X C_X \quad (24)$$

where

$$R_X = 1/g_{m3b1}$$

and

$$C_X = C_{GD3A} + C_{GS5} + C_{GD1a} + C_{DB3a} + C_{DB1a} + C_{GS3b1} + C_{GD3b1} + C_{GD11a} + C_{BD11a} + C_{GD11b} + C_{DB11b} + C_{GD2b} + C_{DB2b}$$

D. Common Mode Gain

In differential amplifiers reported in the literature (e.g. [7], [8].), the common mode and differential mode signals share the same path and have large common mode and differential impedance. For example, in the IRFC OTA, for common mode input, the signal at the gate of M1a and M3a are out of phase. So, as the common mode input decreases, the current in M1a increases and the current in M3a also increases because of out of phase. So, if the small signal current through the M1a is ΔI_d , then current through M3a is $K/a\,\Delta I_d$. Hence, a current of $\left\{\frac{K}{a} - 1\right\}\Delta I_d$ flows from the output node to the cascode node. Hence, the transconductance and output impedance may be shown to be given by (25) and (26).

$$G_m = \frac{I_{out}}{V_{in}} \approx g_{m1a}.(K/a - 1) \quad (25)$$

$$R_{out} = \left(\frac{g_{m7} r_{07} r_{09}}{2}\right) || \frac{g_{m5} r_{05}(r_{01a} || r_{03a})}{2} \quad (26)$$

Hence, the CM gain of IRFC is given by (24)

$$A_{cm,IRFC} \approx g_{m1a}.\left(\frac{K}{a} - 1\right) * \left\{\left(\frac{g_{m7} r_{07} r_{09}}{2}\right) || \left(\frac{g_{m5} r_{05}(r_{01a} || r_{03a})}{2}\right)\right\} \quad (27)$$

The common mode operation of EIRFC is considered next. In the half circuit of EIRFC OTA shown in Fig. 10, the common mode signal sees a lower gain to the source of M5 as the positive feedback loop is not seen by the common mode input. The positive feedback is achieved by the inverting current mirror for differential signals i.e. at the cascode node C differential signals will be seen. However, in case of common mode signals, the current mirror is non-inverting

because, instead of using actual inverters, the signal from the other half of the OTA is used, assuming it is inverted. In the common mode circuit, the current in both the halves are identical so that the currents M5 and M13 add up. As a result, the common mode output impedance is significantly lower than the differential mode output impedance. Hence, the CM gain is reduced by the factor of $g_m r_0$, compared to the IRFC OTA. This in turn improves the common mode rejection ratio. For common mode input, G_m remains the same as that of IRFC.

It can be shown that the output impedance ($R_{out,EIRFC}$) and CM gain ($A_{CM,EIRFC}$) of EIRFC are given by (28) and (29)

$$R_{out,EIRFC} = \frac{r_{05}}{4} \tag{28}$$

$$A_{CM,EIRFC} = g_{m1a}\frac{1}{a}(K-1)(\frac{r_{05}}{4}) \tag{29}$$

From (27) and (29), it is observed that the CM gain of the EIRFC OTA is lesser by a factor of $g_m r_o$ compared to the IRFC OTA.

E. Slew Rate

The Slew Rate (SR) is also enhanced in EIRFC. Both the OTAs are used as unity gain amplifier as shown in Fig. 11 with R1 = 100kΩ, C1 = 1pF and CL = 5.6 pF. It can be found by applying a large transient signal [9], [10], to the non inverting input of the EIRFC assuming a load C_L. In this condition, as the transient signal raises M1a, M1b turns off. As no current flows through M1b, no current flows through M4a and the drain potential of M4a increases. Hence, no current flows through M6, M14 and M2a. The current of $2I_b$ now flows through M2b and is mirrored by K/a times to M3a. The current in M3a splits equally into M5 and M13. The current in M13 is mirrored to the positive output node Vout+ by M15, M17, M8 and M10 whereas the current in M5 flows into the negative output node Vout-. Hence, the slew rate is almost symmetric in EIRFC as compared to the IRFC. The Slew Rate of IRFC OTA for rising and falling edge are I_b/C_L and $5I_b/C_L$ respectively. The Slew Rate of EIRFC OTA for both the edges are $3I_b/C_L$.

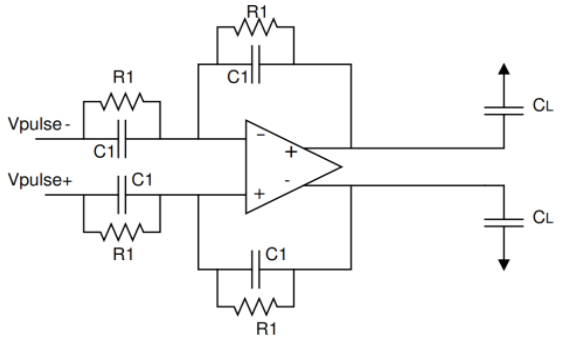

Fig. 11 Circuit for calculation of Slew Rate

V. Simulation Results

The EIRFC OTA and IRFC OTA reported in the literature [6] are simulated using the UMC 90nm CMOS process with a supply voltage of 1.2 volts. The performance is obtained for a load capacitance of C_L. For both the OTAs, the parameter 'K' in the bias current source is assumed to be 3 and 'a' is assumed to be 0.5. The OTAs discussed are implemented and simulated using Cadence SPECTRE Simulator. The area required is the same for all the three OTAs as the transistor widths of M5, M7, and M9 are divided into pairs of M5/M11, M7/M13, M9 and M15. It can be verified from the Table I, that the sizes of M5/M7/M9 are 2 times that of the M5/M13/M7/M15/M9/M17. The improvement in common mode rejection ratio can also be analyzed from the Fig. 13.The various parameters of the OTAs such as DC Gain, UGB, Phase Margin, CMRR, slew rate are given in Table II. The Figure of Merit [5] [FoM] given by (30) is also computed and given in Table II.

$$FoM = Slew\ Rate * C_L/I_{bias}\{\left(\frac{V}{us}\right)p_f)/mA\} \tag{30}$$

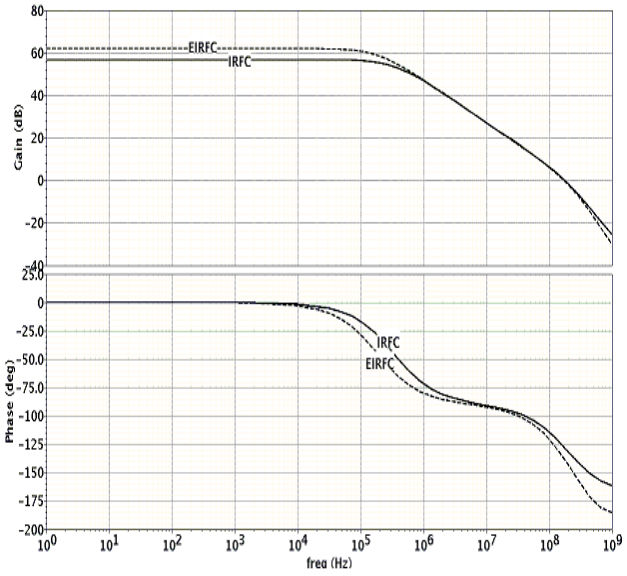

Fig. 12 Gain and Phase plot of EIRFC and IRFC OTAs

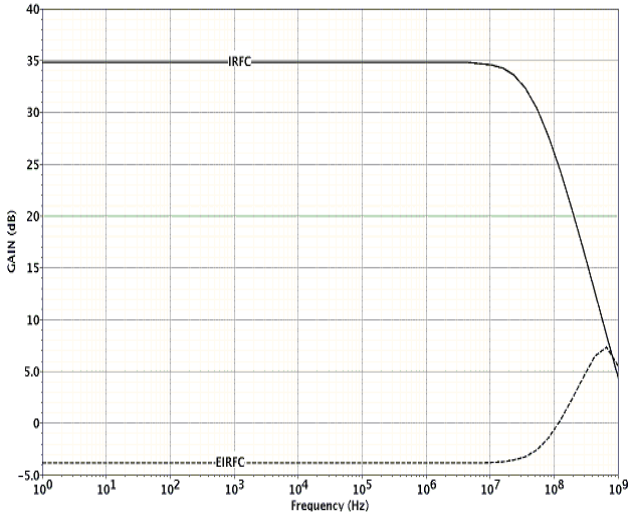

Fig. 13 CM gain of EIRFC and IRFC OTAs

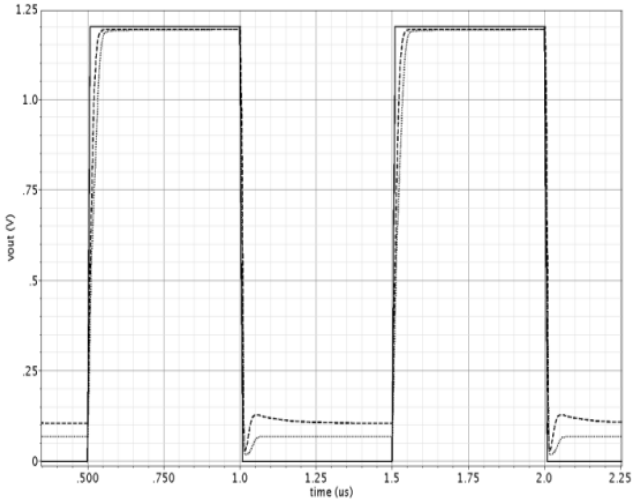

Fig. 14 Slew rate of IRFC and EIRFC OTA

TABLE I
DEVICE SIZE OF EIRFC AND IRFC OTAS

DEVICE	EIRFC	IRFC
M0	276/0.35	276/0.35
M1a/M1b/M2a/M2b	67.6/0.35	67.6/0.35
M3a/M4a	80/0.5	80/0.5
M3b/M4b	12.1/0.5	12.1/0.5
M3c/M4c	12.1/0.5	12.1/0.5
M5	10.5/0.18	21/0.18
M13	10.5/0.18	-
M7	8.0/0.18	16.1/0.18
M15	8.0/0.18	-
M9	24.0/0.5	48.0/0.5
M17	24.0/0.5	-
M11a/M12a	4.5/0.18	4.5/0.18
M11b/M12b	4.5/0.18	4.5/0.18

TABLE II
COMPARISON OF THE PERFORMANCE METRICS OF EIRFC AND IRFC OTAS

Parameter	EIRFC	IRFC
Power Consumption	672uW	672uW
DC Gain	62dB	56dB
CM Gain	-4dB	34dB
CMRR	66	22
Load Capacitance(C_L)	5.6pF	5.6pF
Phase Margin (PM)	50	55
GBW[MHz]	164	164
Average Slew Rate (V/μS)	39.3	26.2
Settling time 1%(nS)	13.8	15.3
FoM	393	262

From Figs. 12-14 and Table II, the following observations may be made:

- The DC gain of the EIRFC OTA is higher by 6dB compared to that of IRFC OTA.
- The settling time is lower by 1.5ns for EIRFC.
- The Slew rate and Figure of Merit of EIRFC OTA are higher by a factor of 1.5 compared to that of IRFC.

VI. CONCLUSION

The fully differential enhanced IRFC OTA proposed in this paper and the IRFC OTA reported in the literature have been designed and simulated in UMC 90nm CMOS technology. The increase in the low frequency DC gain is achieved by positive current feedback technique. The proposed OTA results in higher slew rate. For improvement in the PM of the EIRFC OTA, a feed forward capacitor can be added across the cascode transistor. Due to its lower CM gain compared to the IRFC OTA, it results in high common mode rejection ratio.

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