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Internal Node Stabilization for Voltage Sense Amplifiers in Multi-Channel Systems

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***Abstract*—**This paper discusses the undesirable charge transfer by the parasitic capacitances of the input transistors in a voltage sense amplifier. Due to its intrinsic rail-to-rail voltage transition, the input sides are inevitably disturbed. It can possible disturb the stabilities of the reference voltage levels. Moreover, it becomes serious in multi-channel systems by altering them for other channels, and so degrades the linearity of the systems. In order to alleviate the internal node voltage transition, the internal node stabilization technique is proposed by utilizing an additional biasing circuit. It achieves 47% and 43% improvements for node stabilization and input referred disturbance, respectively.

***Keywords*—**Voltage sense amplifier, voltage transition, node stabilization, and biasing circuits.

I. Introduction

VOLTAGE sense amplifiers are widely used circuit blocks to generate firm decisions from a meaningful input analog signals. There are lots of different types of voltage sense amplifiers, and they are widely used in various fields such as memories, display driver, data converters, communication transceivers, and so on [1]-[4].

Each structure has its own advantages and disadvantages. Depending on the existence of static currents, voltage sense amplifiers can commonly be divided into two categories. First, the static voltage sense amplifiers use the static biasing current, and so its power consumption is high and probably not tolerable in nowadays mobile environment. On the other hand, the dynamic latch-type voltage sense amplifier can save its power consumption because it breaks the current path during the reset phase. Due to its high power efficiency and rail-to-rail output swing, the dynamic latch-type voltage sense amplifier gains more popularity nowadays. However, its full-scale output swing can possible create unacceptable input-referred disturbance through the inevitable parasitic capacitances. The node stabilization technique is proposed in the paper to reduce the input referred disturbance.

This paper is organized as follows: Section II introduces and compares the popular dynamic latch-type voltage sense amplifiers to show their pros and cons. The sources of node disturbance are explained. The node stabilization technique and design procedures are presented in Section III. The conclusions are shown in Section IV.

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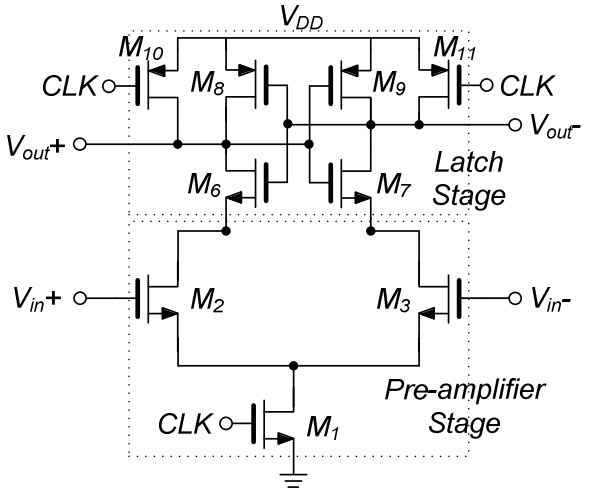

Fig. 1 A dynamic latch-type voltage sense amplifier

II. Consideration of Node Disturbance

A. Stacked Dynamic Latch-Type Voltage Sense Amplifier

The typical structure of a dynamic latch-type voltage sense amplifier is shown in Fig. 1 [5], [6]. A dynamic latch-type voltage sense amplifier consists of pre-amplifier in the bottom and dynamic latch stages in the top. Its operation is solely controlled by the CLK signal, and exhibits two distinguished reset and decision phases. During the reset phase, the CLK becomes low so that transistors M_{10} and M_{11} clamp the output nodes of the pre-amplifier stage to VDD. The tail current source transistor M_1 turns off, shutting down the current path. It is noted that the common source node in the pre-amplifier stage is floating and depends on the higher voltage level of two input node. As the CLK goes high, the M_1 turns on and reconstructs current paths. Thus, a meaningful input differential signal is amplified by the pre-amplifier stage, and transferred to the latch stage. Then, the positive feedback dynamic latch stage differentiates further to the supply voltage levels at the output nodes. This structure has become popular due to its rail-to-rail output swing as well as the absence of the static current.

Despite of numerous advantages of the dynamic latch-type voltage sense amplifier in Fig. 1, the direct coupling between the pre-amplifier and latch stages can possibly create a serious input referred disturbance or noise. This input noise becomes more critical in multi-channel system because it manipulates the reference voltage levels that can possible result in a wrong decision in neighborhood channels. The input referred

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disturbance due to full scale outputs can be mitigated by separating the structure.

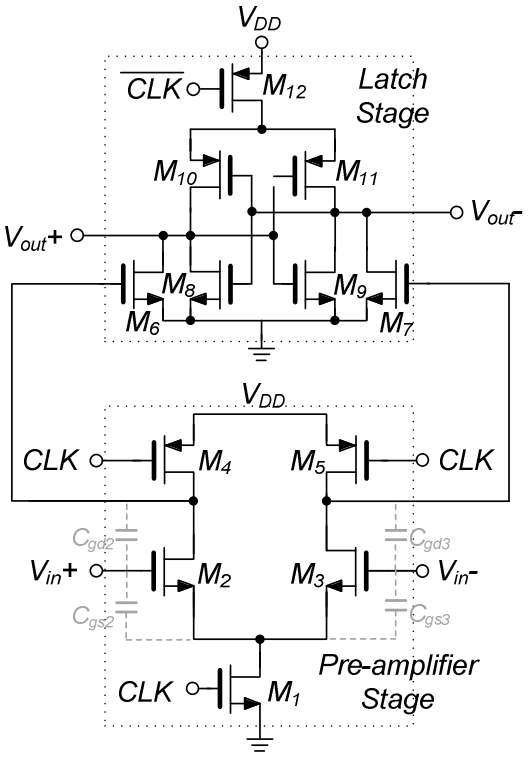

Fig. 2 A double-tail voltage sense amplifier

B. Double-Tail Dynamic Latch-Type Voltage Sense Amplifier

A double-tail voltage sense amplifier showsthe lower input referred disturbance by separating the pre-amplifier stage and dynamic latch stages in Fig. 2 [7]. Moreover, its separating structure seems more applicable to low voltage deep sub-micron CMOS technologies. The intermediate transistors M_6 and M_7 are inserted to transfer the signals from the pre-amplifier to the dynamic latch stages, and also mitigate the abrupt disturbance from the dynamic latch-type stage to the pre-amplifier stage. However, the input referred disturbance may be insufficiently suppressed even in the double-tail dynamic latch-type voltage sense amplifier in Fig. 2 for the multi-channel systems.

There are two main sources that transfer the internal voltage fluctuations into the input sides, resulting in inevitable input disturbance. First, the parasitic gate-source capacitances $C_{gs2}$and C_{gs3} of the differential pair in the pre-amplifier stage create the input referred noise. As mentioned earlier, the common source node of the differential pair is floating during the reset phase. When the CLK goes high, M_1 should reconstruct the current path and the common source node of the differential pair should drop to ground immediately. Then, a large amount of charge is interacted with the input nodes through C_{gs2} and C_{gs3}, and then the input referred disturbance generates. Moreover, the input differential pair transistors M_2 and M_3 have different capacitance sizes of C_{gs2} and C_{gs3} because the differential voltage levels are applied to the differential input nodes. Thus, different amounts of the input referred disturbance can possible worsen the conversion linearity. The other sources of the input referred noise are the gate-drain parasitic capacitances C_{gd2} and C_{gd3} of the input differential pair in Fig. 2. The charge transfer through the C_{gd2} and C_{gd3} mainly results from the dynamic latch operation. The rapid voltage divergence at the output nodes can affects the input nodes. Especially when the positive feedback in the dynamic latch is not sufficiently strong, the unbalanced voltage fluctuation is leaked to the input sides through the C_{gd2} and C_{gd3}, so that it may have a chance to invert the final decisions, degrading the overall system performance.

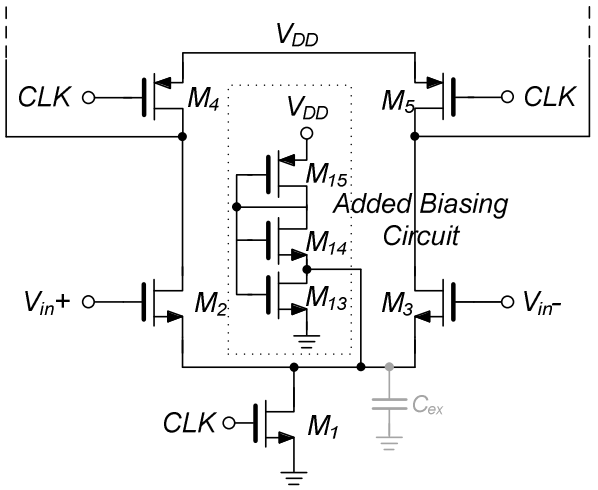

Fig. 3 Internal node stabilization technique using added biasing circuits in the pre-amplifier stage

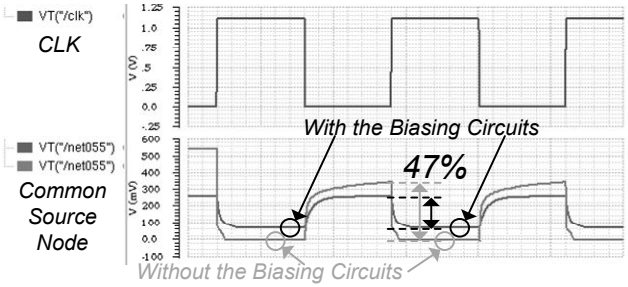

Fig. 4 The effect of the proposed added biasing circuits on suppressing the voltage fluctuation in the common source node of the pre-amplifier stage

III. Node Stabilization Technique

A. Node Stabilization Technique

The input referred disturbance at the input nodes in Fig. 2 is alleviated by suppressing the voltage fluctuation at the common source node of the input differential pair. One remedy is to place an external capacitor C_{ex} to the ground, as shown in Fig. 3. This method is very simple. However, it can seriously slow down the decision speed. The proposed method is to intentionally control the voltage level at the common source node so that the voltage fluctuation is suppressed. In order to do that, an added biasing circuit is inserted, as shown in Fig. 3. The

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added biasing circuit prevents the common source node of the differential pair from dropping to the ground even when the CLK goes high. Therefore, the voltage fluctuation is suppressed and the amount of input referred disturbance is reduced.

TABLE I
RELATIONSHIP BETWEEN VOLTAGE RATIO AND SIZE RATIO

Voltage Ratio, $\left(\frac{V_{OV}}{V_{Target}}\right)$	Size Ratio, $\frac{\left(W/L\right)_{13}}{\left(W/L\right)_{14}}$
1/2	1/8
1	1/3
2	4/5
4	16/9

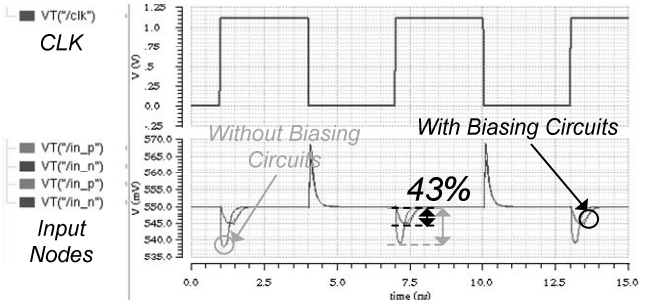

Fig. 5 The effect of the proposed added biasing circuits on suppressing the input referred disturbance in the pre-amplifier stage

The effects of the proposed added biasing circuit on suppressing the voltage fluctuation in the common source node of the pre-amplifier stage is simulated and shown in Fig. 4. The voltage fluctuation with the added biasing circuit decreases by 47%, compared to the voltage fluctuation without the biasing circuit. The effects of the proposed added biasing circuit on suppressing the input referred disturbance is simulated and shown in Fig. 5. The voltage fluctuation at the input nodes with the added biasing circuit decreases by 43%, compared to the voltage fluctuation without the biasing circuit. Note that the resistance and capacitance at the input sides are modified to exaggerate the input referred disturbance in the simulations. Due to the added biasing circuit, the voltage level of the common source node at the pre-amplifier stage does not perfectly drop to ground during the decision phase. Nevertheless, the static current path still does not exist in Fig. 3 during the decision phase because the current source transistor M_1 stay in the deep sub-threshold operation.

Another source of the input referred disturbance is the gate-drain parasitic capacitance C_{gd2} and C_{gd3} of the input differential pair. Since the output nodes of the pre-amplifier stage are clamped to VDD during the reset phase and diverge to the supply levels during the decision phase, its abrupt large voltage transition is coupled to the input sides through C_{gd2} and C_{gd3} and results in the input referred disturbance. It is known that a neutralization technique is somewhat effective to suppress the input referred disturbance resulting from C_{gd2} and C_{gd3} [8], [9]. In the double-tail voltage sense amplifier, the intermediate transistors M_6 and M_7 play an important role by isolating the pre-amplifier stage from the dynamic latch-type stage. Thus, the neutralization technique does not seem so effective in the double-tail voltage sense amplifier.

B. Design of the Biasing Circuits

An added biasing circuit in Fig. 3 can basically be an arbitrary circuit that can generate the certain voltage level. A current mirror structure is very simple to satisfy the design goal. However, it is very difficult to get the precise controllability as well as an arbitrary voltage level without additional branch which adds more power consumption. The *sooch* cascode current mirror is adopted in Fig. 3 [10], [11]. In this structure, the voltage level can be easily controlled by the transistor size ratio betweenM_{13} and M_{14}. Since M_{14}always makes M_{13} operate in the triode region, their size ratio m is defined by

$$m = \frac{\left(\frac{W}{L}\right)_{13}}{\left(\frac{W}{L}\right)_{14}} = \frac{\left(\frac{V_{OV}}{V_{Taget}}\right)^2}{2\left(\frac{V_{OV}}{V_{Taget}}\right)+1}, \quad (1)$$

where W, L, and V_{OV} denote the width, length and overdrive voltage of a given transistor. The desired voltage level is denoted by V_{Target} in (1). The relationship between m and the voltage ratio V_{OV}/V_{Target} is illustrated in Table I.

IV. CONCLUSIONS

The input referred disturbance problems of voltage sense amplifiers are discussed. Due to the parasitic capacitances, the voltage fluctuation of the internal nodes are transferred to the input sides and shown in the form of unwanted disturbance. The presented added biasing circuit is effective to stabilize the internal node to suppress the voltage fluctuation. The 47% and 43% of improvements for the node stabilization and the input referred disturbance are shown in simulations.

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