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Design and Implementation of Quantum Cellular Automata Based Novel Adder Circuits

Santanu Santra, Utpal Roy

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***Abstract*—**The most important mathematical operation for any computing system is addition. An efficient adder can be of greater assistance in designing of any arithmetic circuits. Quantum-dot Cellular Automata (QCA) is a promising nanotechnology to create electronic circuits for computing devices and suitable candidate for next generation of computing systems. The article presents a modest approach to implement a novel XOR gate. The gate is simple in structure and powerful in terms of implementing digital circuits. By applying the XOR gate, the hardware requirement for a QCA circuit can be decrease and circuits can be simpler in level, clock phase and cell count. In order to verify the functionality of the proposed device some implementation of Half Adder (HA) and Full Adder (FA) is checked by means of computer simulations using QCA-Designer tool. Simulation results and physical relations confirm its usefulness in implementing every digital circuit.

***Keywords*—**Clock, Computing system, Majority gate, QCA, QCA Designer.

I. Introduction

CURRENTCMOS technology is on verge of reaching the bound of feature size reduction. Its high power consumption also prevents the energy-efficient realization of complex logic implements at nano-scale. Also, downsizing of CMOS circuitry does not necessarily produce corresponding gains in device density [1]. One conventional way to enhance the performance of logic system is parallelism [2].Quantum-dot Cellular Automata (QCA) is the alternatives to conventional CMOS technology for producing high computational power and compact density for the digital circuits and gives at nano-scale level. QCA also have the ability for a new method of computation and information transformation [3], [4]. As there are not any current in the circuit and output capacity QCA power consumption is extremely lower than CMOS. The two important gates in QCA technology are three input majority and inverter gate. In this paper, half adder and full adder circuits are designed using proposed XOR gate. Both half adder and full adder is implemented using one layer QCA designer.

The organization of the rest of paper is as follows. Section II discusses the QCA and its principals. Section III describes two novel XOR gates and comparative study of most recent XOR gates approach. Novel design of half adder, full adder and comparative study of most recent full adder designs are presented in Section IV. Finally, Section V concludes the article.

S.Santra is with Department of Computer Science & Engineering, Bengal Institute of Technology and Management, Santiniketan-731236, West Bengal, India (phone: 9474895712; e-mail: santrasantanu@gmail.com).

U. Roy is with Department of Computer & System Science, Visva-Bharati University, Santiniketan-731235, West Bengal, India (e-mail: roy.utpal@gmail.com).

II. Quantum Dot Cellular Automata

The principal of Quantum Cellular Automata was been proposed for implementing classical cellular automata by systems designed with the help of quantum dots [4], as a replacement for classical computing using CMOS technology. A QCA is a planner array of quantum cells [5]. QCA emerged as a new paradigm to encode binary information in the charge configuration within a cell. Coulomb interaction [6] in between cells is sufficient to accomplish the computation in QCA arrays, as a result no interconnect wires are needed between cells. Also no current flows out of the quantum cell so that low power dissipation is inverted.

A. Basic QCA Device

QCA technology is based on the interaction of bi-stable QCA cells design from four quantum dots. A schematic diagram of a basic cell structure is shown in Fig. 1 (a). The cell is charged with two free electrons by tunneling between adjacent dots. These electrons tend to occupy antipodal sites as a result of their mutual electrostatic columbic repulsion. Thus, there exist two equivalent energetically minimal arrangements of the two electrons in the QCA cell, as shown in Figs. 1 (b) and (c). These two types of cell polarization represent logic "0" and logic "1" binary information, encoded in the charge configuration of the QCA cell [7].

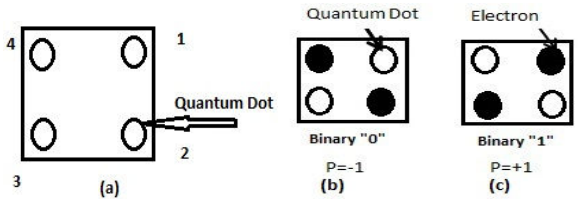


Fig. 1 Basic QCA Cell and binary encoding (a) Schematic of the basic cell constructed from 4 quantum dots (b) Binary 0 (P=-1) (c) Binary 1 (P=+1)

Coulomb repulsion causes the electrons to occupy antipodal sites; the ground level charge distribution may have the electrons aligned along either of two diagonal axes shown in Figs. 1 (b) and (c). Cell polarization (define in (1)) of a QCA cell has been calculated as a quantity which measures the extent to the charge distribution is aligned along one of these axes [4].

$$\frac{(\rho 2+\rho 4)-(\rho 1+\rho 3)}{\rho 1+\rho 2+\rho 3+\rho 4} \quad (1)$$

where ρ_i denotes the electronic charge at dot i. According to (1), electrons exactly localized on position two and four produced P="+1", electrons on positions one and three produced P="-1" as cell charge and the respective binary encoded values are "1" while cell polarized P="+1" and "0" while cell polarized P="-1" Figs. 1 (b) and (c) represent the corresponding representation.

B. QCA Based AND, Inverter, and Wires Circuits

In Quantum Cellular Automata, elementary Boolean logic functions can be realized by exploiting the physical interaction between cells. The fundamental QCA logic device including QCA Majority gate (Fig. 2), QCA Inverter (Fig. 3) and QCA wire (Fig. 4) [4]-[8] are described as bellow.

1. QCA Majority Gate

Majority gate consist of only 5 QCA cells [4], 3 input cells, one intermediate cell and one output cell, (2) shows the functionality of a Majority gate. A two input AND function can be implemented by a three input majority gate by fixing one of its inputs as logic zero whereas if one input of a majority gate set to logical one it acts like a two input OR function [9]. Figs. 5 (a) and (b) show the functionality of AND and OR gate respectively.

$$m(A, B, C) = A.B + B.C + A.C \quad (2)$$

2. QCA Inverter Gate

Two standard cells in a diagonal orientation are geometrically similar to two rotated cells in a horizontal orientation; as a result standard cells in a diagonal orientation tend to align in opposite polarization direction as in the inverter chain. This ant aligning behavior can be used in designing a QCA inverter Fig. 3 shows the basic diagram of a QCA inverter circuit. The "information" is propagating from left to right.

3. QCA Wire

In a QCA wire, the binary information propagates from input to output because of the Columbic interactions between quantum cells, which is a result of the system attempting to settle to a ground state. Any cells along the wire that are anti-polarized to the input would be at a higher energy level and would soon settle to the correct ground state. The propagation in a 90-degree QCA wire is shown in Fig. 4. There is also a 45-degree QCA wire can also be used to design any QCA circuit where the propagation of the binary information alternates between the polarizations.

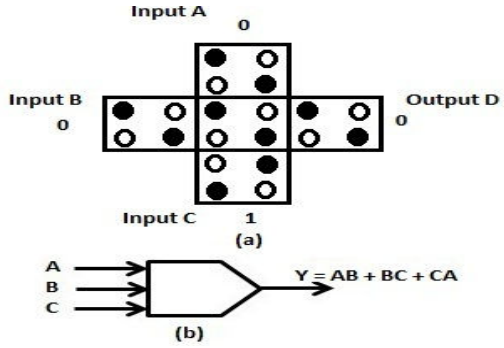


Fig. 2 Basic Majority Gate (a) Schematic representation of Majority Gate (b) QCA Symbol of Majority Gate

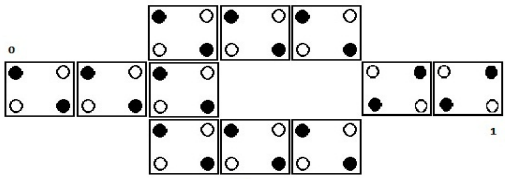


Fig. 3 QCA Inverter Circuit

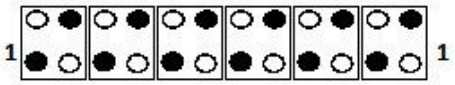


Fig. 4 QCA Wire

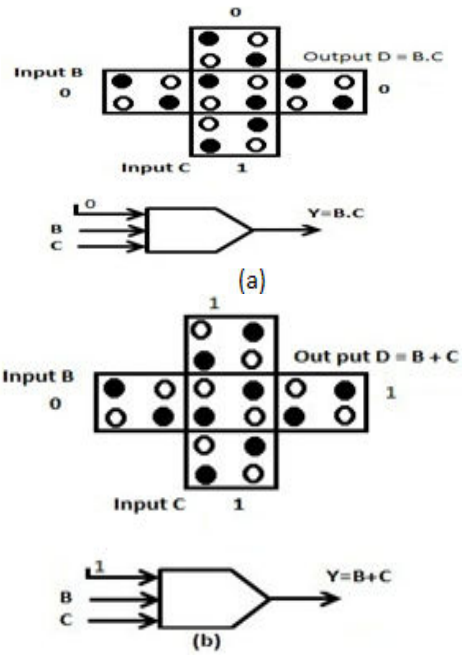


Fig. 5 Primitive Components of QCA (a) AND Gate Representation using Majority Gate quantum dots (b) OR Gate Representation using Majority Gate

4. QCA Clock

The QCA clock [10] is accomplished by controlling the potential barriers between adjacent quantum-dots. When the potential is low the electron wave functions become delocalized resulting in no definite cell polarization. Raising

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the potential barrier decreases the tunneling rate, and thus, the electrons begin to localize. As the electrons localize, the cell gains a definite polarization. When the potential barrier has reached its highest point, the cell is said to be latched. Latched cells act as virtual inputs and as a result, the actual inputs can start to feed in new values. This enables easy pipelining of QCA circuits. It has been shown that four clocking zones each Π/2 degrees out of phase is all that is required by any QCA circuit. Fig. 6 shows four clocking phases and the related polarization of electrons in these phases. During the first clock phase (Switch) QCA cells begin un-polarized and their inter-dot potential barriers are low. In this phase barriers are high enough to suppress any electron tunneling. In the next (hold) phase the outputs of subgroup can be used as inputs to the next stage. In third phase (release) barriers are lowered and cells are allowed to relax to an un-polarized state. Finally in last phase (relax), cell barriers remain lowered and cell remain un-polarized state [4].

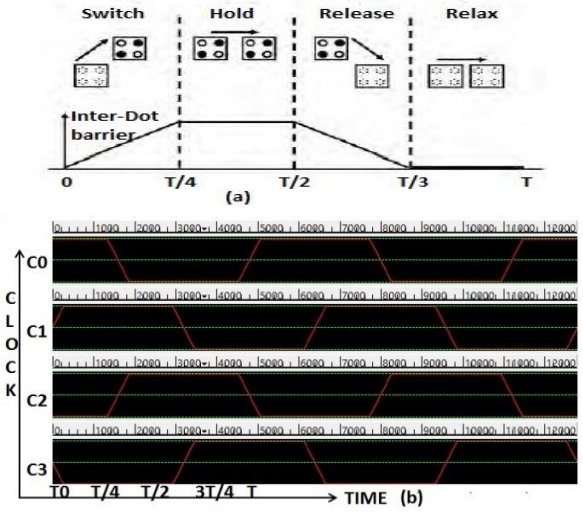


Fig. 6 QCA clock (a) Four phase of operation of QCA cells during a clock period (b) Four phase QCA clocking scheme

III. QCA Implementation

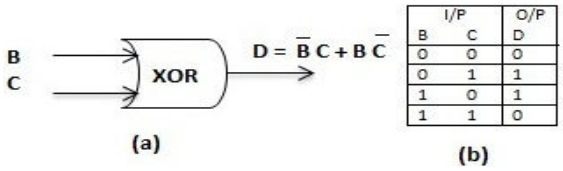
The basic logic gate AND and OR can be implemented using majority gate by fixing the polarization to one of the inputs as P=-1 (Binary0) or P=+1 (Binary1). The NAND function can be implemented by connecting AND gate followed by an inverter circuit. Similarly NOR function is realized by connecting OR gate followed by an inverter.

A. QCA Implementation of XOR Gate

Digital circuits can be implemented by using basic logic gates like AND, OR and NOT, also universal gates NAND and NOR can be used. In addition of these gates Exclusive-OR (XOR) and Exclusive-NOR (XNOR) are also used. To design any arithmetic circuit and complex circuit XOR and XNOR gates are useful, since these gate are complex to fabricate with hardware usually ground as two input gates.

The XOR function performs the following logic operation. The operational function of XOR gate can be represented as in (3).

$$A \oplus B = \overline{A}.B + A.\overline{B} \quad (3)$$



I/P		O/P
B	C	D
0	0	0
0	1	1
1	0	1
1	1	0

Fig. 7 XOR Gate (a) Schematic XOR Gate (b) Truth Table

The representing symbol and the truth table of XOR gate is shown in Fig. 7. In digital logic XOR is a logical value depending on the two inputs and the logical value of XOR is true only if odd numbers of inputs are true otherwise the logical value is false. This forms a fundamental logic gate in many operations to follow. In digital logic if the specific type of gate is not available then it may be constructing by other available gates. An XOR gate can be trivially constructed from the basic gate AND, OR and NOT gates. However, the approach represent in Fig. 8 requires five gates of three different kinds.

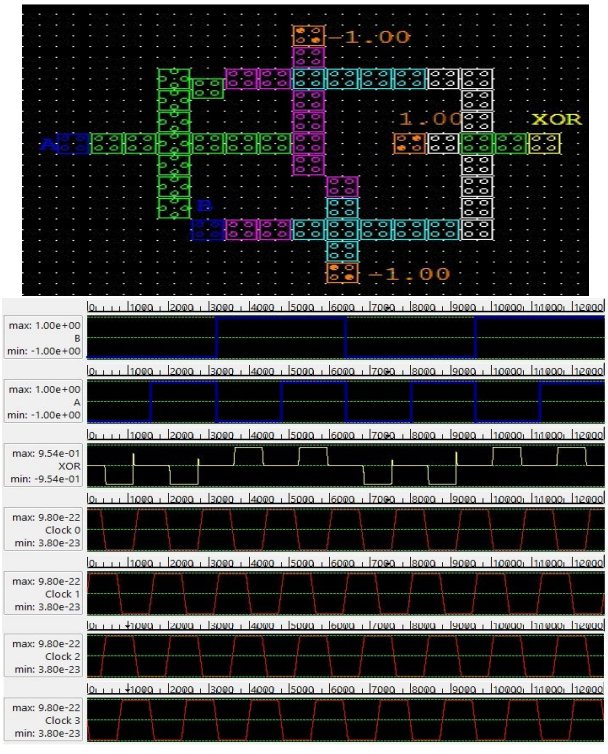


Fig. 8 Proposed XOR Gate1 (a) Schematic XOR Gate using QCA cells (b) Simulation result of XOR Gate

The Boolean function represented in equation 4 is also another one representation of XOR gate, that is implemented using QCA Designer [11] and the simulated circuit and the simulation result is shown in Fig. 9.

$$A \oplus B = (A + B).(\overline{A.B}) \quad (4)$$

XOR is a logical operation on two operands and the result is logically true if and only if odd numbers of inputs are true otherwise it result as logically false. XOR function can be constructed using AND, OR and NOT gates. For instances it can also be constructed by using universal gate NAND and NOR. Fig. 8 shows the proposed XOR gate designing using the QCA cells.

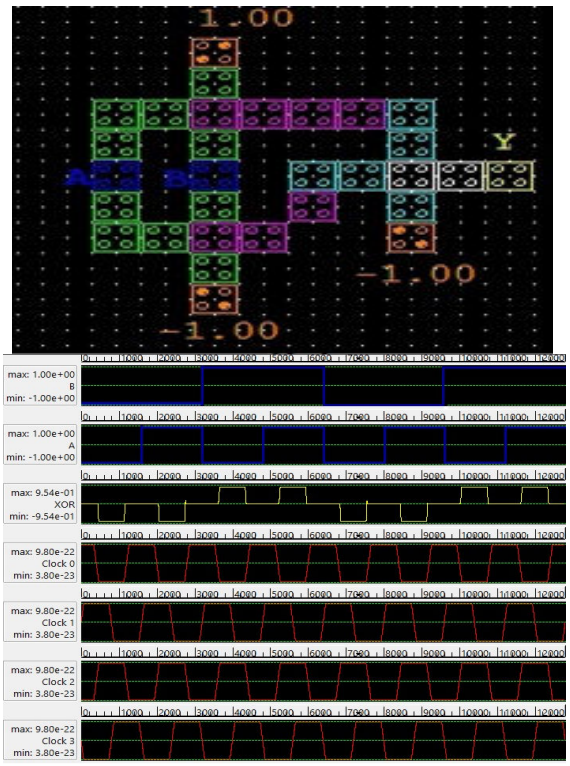


Fig. 9 Proposed XOR Gate2 (a) Schematic XOR Gate using QCA cells (b) Simulation result of XOR Gate

B. Comparative Study of QCA XOR Gates

Proposed circuit layout and functionality checking, a simulation tool for QCA circuits QCA Designer [11] version 2.0.3, is used. The following parameters are used for a bitable approximation: cell size=18nm, clock high=9.800000e-022 J, clock low=3.800000e-023 J, Dot diameter=5nm, Space between two cells = 2nm. Most of the mentioned parameters are default values in QCA Designer. Recent literature shows the possible QCA implementations have cell sizes of 3nm [12], 2.8nm [13] and 1.32nm [14]. In [15] a 25nm cell size was used there should be a limit on the maximum cells in a clock zone.

Table I gives the comparison of proposed design with several previous designs [18]-[20]. It is evident from Table I that the proposed designs are efficient in terms of cell count, majority gate, delay, and area to simulate circuits.

TABLE I
COMPARATIVE STUDY OFPROPOSED DESIGN WITH SOME MOST RECENT DESIGN LAYOUTS

XOR		Cells	Majority gates	Delay	Area (nm^2)		
					Total	Use	% of use
As in [15]	a	41	3	4	35640	13284	37.27
	b	55	4	4	60588	17820	29.41
	c	62	4	4	57024	20088	35.22
As in [16]	a	34	4	4	25920	11016	42.50
	b	54	3	4	51840	17496	33.75
	c	52	4	4	50544	16848	33.33
	d	52	4	4	50544	16848	33.33
	e	48	3	3	35640	15552	43.63
	f	54	3	4	48600	17496	36.0
	g	42	3	3	29160	13608	46.66
As in [17]		58	3	3	2808	50544	18792
Proposed	a	51	4	5	58320	16524	28.33
	b	30	3	4	28044	9720	34.66

IV. ADDER DESIGN

The major arithmetical operations can be implemented by using adder circuit; adder circuit is classified as Half Adder (HA) and Full Adder (FA). In this section we implemented HA and FA by using the proposed XOR gate.

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A. QCA Half Adder (HA) Using Proposed XOR Gate

Half adder is a combinational circuit which performs addition of two operand bits. When two inputs operand are added, the SUM and Carry outputs are produce according to the truth table. The proposed XOR circuit is applied to implement a QCA half-adder. To implement the Half Adder circuit we use the novel XOR gate and one majority gate which are used as AND gate. Here a one bit half circuit is implemented, which can be defined as follows:

Inputs: two operand bits A and B.
*Outputs:*Sum and Carry_Out.

The output of half adder circuit is represented in (5) and (6).

$$\text{Sum} = \text{A} \oplus \text{B} \tag{5}$$

$$\text{Carry_Out} = (\text{A}.\text{B}) \tag{6}$$

Fig. 10 (a) shows the QCA layout of half adder circuit and Fig. 10 (b) shows the simulation result of half adder circuit.

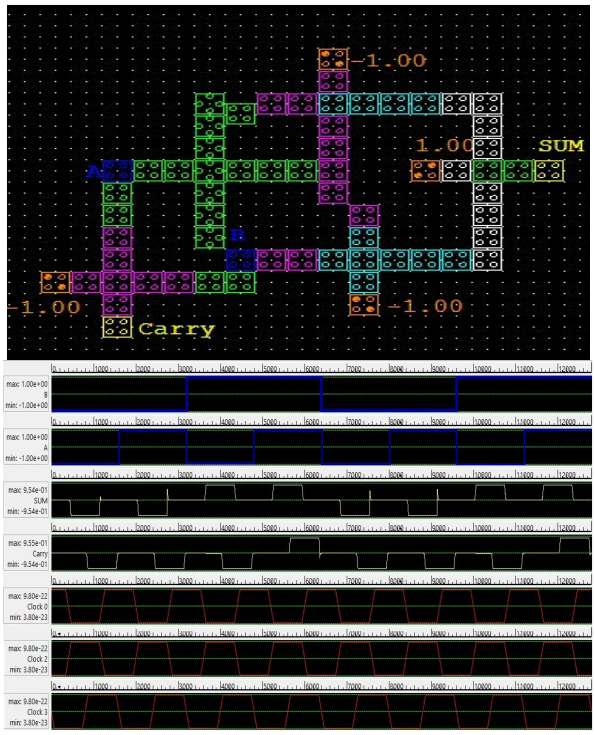


Fig. 10 Half Adder (a) Schematic Half Adder using Proposed XOR gate and Majority Gate (b) Simulation result of Half Adder Circuit

B. 1 Bit QCA Full Adder (FA) Using Proposed XOR Gate

Full adder circuit can be implemented using digital logic gates. When three inputs A, B, Carry-in are added, the Sum and Carry-out output are produced according to the truth table. Here we have designed the full adder circuit using the proposed XOR gate. To implement the complete circuit of a one bit full adder we use 2 numbers of XOR gate and 3 numbers of majority gates where two are used as AND gate and one is used as OR gate. Here a one bit full adder circuit is implemented, which can be defined as follows:

$$Sum = A \oplus B \oplus C \tag{7}$$

$$\text{Carry_Out} = (\text{A}.\text{B}) + (\text{A} \oplus \text{B}).\text{C} \tag{8}$$

The output of full adder circuit is representing in (7) and (8). Fig. 11 (a) shows the QCA implementation of full adder and Fig. 11 (b) shows the simulation result of full adder circuit.

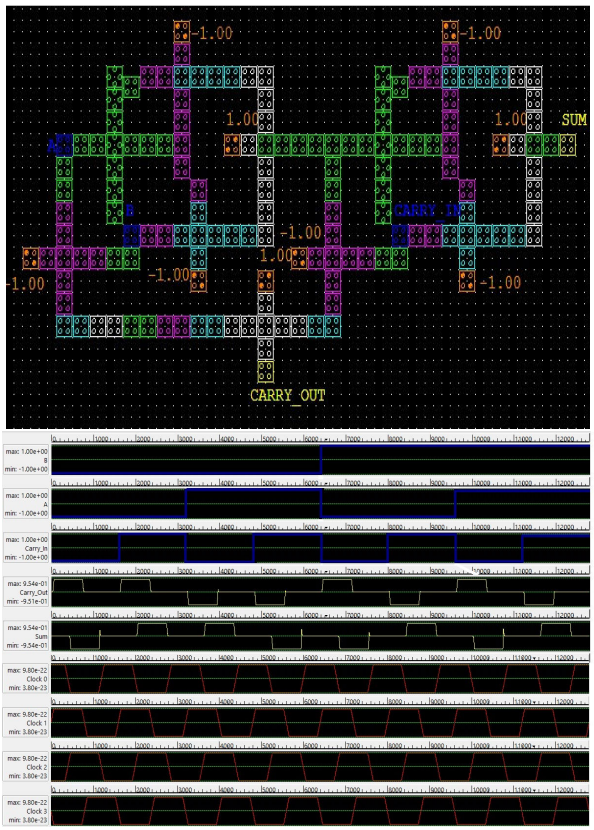


Fig. 11 Full Adder (a) Schematic Full Adder using Proposed XOR gate and Majority Gate (b) Simulation result of Full Adder Circuit

C. Result Analysis

In this study we implement Half Adder and Full Adder Circuit using XOR gate only. The novelty of the XOR gate besides parameter like delay, majority gate, area are minimal in comparison to other design as proposed in the literature [4], [18]-[22].The complexity parameters such as cell count, timedelay and area consumption of QCA circuit has been calculated with QCA designer [20]. Attempt has been taken to design a QCA adder circuit with the proposed XOR gate only.

The comparison between various parameter of the circuit such as no. of cell count, time delay and total area consumption with the work available in literature has been compared.

Complexity in terms of cell counts, delay and area consumption of QCA circuits can be easily obtained by QCA Designer. Table II demonstrates the comparison between the

QCA based full adder implementation with proposed XOR gate and the results available in literature [4], [18]-[22]. The results indicate that number of cell count is considerably low in our design. The design made in [20] has been made in pedestrian way with various basic gates. But the present design has been completed with three XOR gates only.

TABLE II
PARAMETER COMPARISONS OF PRESENT QCA FULL ADDER DESIGN WITH THE RESULTS AVAILABLE IN LITERATURE [4], [18]-[22]

Full Adder	No. of cells	Delay (clock cycle)	Total area(μm^2)
FA as in Paper[4]	192	NA	0.20
FA as in Paper [18]	292	3.5	0.62
FA as in Paper [19]	145	1.25	0.17
FA as in Paper [20]	108	1	0.10
FA as in Paper [21]	135	1.25	0.14
FA as in Paper [22]	220	3	0.36
Proposed FA using XOR	150	2.25	0.28

V. CONCLUSION

This article represents the design, layout and simulation of combinational circuits based on novel XOR circuit configuration. An optimal design for XOR base half adder and full adder circuits has been proposed. The proposed circuits are simulated using QCA based circuits simulation tools i.e. QCA Designer [23]. This design is efficient in terms of cell count, area. Moreover considering the less numbers of cell count can presume that power consumption in such a circuit will obviously be low.

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