Pattern Recognition Using Feature Based Die-Map Clusteringin the Semiconductor Manufacturing Process

Seung Hwan Park, Cheng-Sool Park, Jun Seok Kim, Youngji Yoo, Daewoong An, Jun-Geol Baek

Abstract—Depending on the big data analysis becomes important, yield prediction using data from the semiconductor process is essential. In general, yield prediction and analysis of the causes of the failure are closely related. The purpose of this study is to analyze pattern affects the final test results using a die map based clustering. Many researches have been conducted using die data from the semiconductor test process. However, analysis has limitation as the test data is less directly related to the final test results. Therefore, this study proposes a framework for analysis through clustering using more detailed data than existing die data. This study consists of three phases. In the first phase, die map is created through fail bit data in each sub-area of die. In the second phase, clustering using map data is performed. And the third stage is to find patterns that affect final test result. Finally, the proposed three steps are applied to actual industrial data and experimental results showed the potential field application.

Keywords—Die-Map Clustering, Feature Extraction, Pattern Recognition, Semiconductor Manufacturing Process.

I. INTRODUCTION

THE importance of big data analysis in the semiconductor industry is growing increasingly, as the semiconductor manufacturing process produces core products that are more integrated. Also, because of the high demand for the newest electronic devices, such as smart phones and tablets, it is important to improve the product yield through state-of-the-art equipment or process management techniques. The steps in semiconductor manufacturing are complicated because there are hundreds of manufacturing processes which take several months to complete. Therefore, to effectively manage the process, semiconductor manufacturing companies require a super-clean environment, regular equipment maintenance and comprehensive worker training [1].

In particular, big data analysis is essential for process management for the process management. This study focuses on analysis of data generated during the test process called as post-fabrication process. In general, test data analysis is performed usingtest data in die level and it is important to find a

Seung Hwan Park, Jun Seok Kim, Cheong-Sool Park, and Youngji Yoo are with the School of Industrial Management Engineering, Korea University, Anam-dong, Seongbuk-gu, Seoul, 136-713, Republic of Korea (phone: 82-02-925-5035; e-mail: {udongpang, bliths, dumm97, kakiro}@korea.ac.kr).

Daewoong An is with DRAM Development Division, SK Hynix Semiconductor, Gyeongchung-daero 2091, Bubal-eup, Icheon, Gyeonggi-do, 467-701, Republic of Korea (phone: 82-031-630-4114; e-mail: daewoong.an@sk.com).

Jun-Geol Baek is professor in the School of Industrial Management Engineering, Korea University, Anam-dong, Seongbuk-gu, Seoul, 136-713, Republic of Korea (phone: 82-02-3290-3396; e-mail: jungeol@korea.ac.kr).

relationship to test data and the final test results. Fig. 1 represents the overall flow chart of semiconductor manufacturing process.

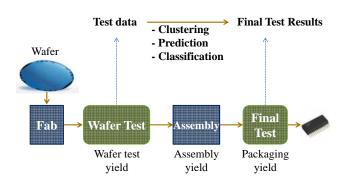


Fig. 1 Flow chart of thesemiconductor manufacturing process

The semiconductor manufacturing process consists of fabrication and post fabrication process. In Fig. 1, Fab means stage that fabricates wafers and the subsequent process consists of a wafer test, the assembly, and the final test [2]. In conjunction with each of these steps, the fabrication yield, the wafer test yield, the assembly yield and the packaging yield are all calculated. The fabrication yield refers to the ratio of wafers in to wafers out. The wafer test yield is calculated as the ratio of whole chips of wafer out and the number of non-defective chips as decided by the wafer test. The assembly and packaging yields are the ratio of the input chips after assembly and the input chips after the final test respectively. This study focuses primarily on analysis of final test results using feature based clustering from test data from the wafer test.

In order to best improve the yield in the semiconductor manufacturing process, many researches have been performed for a long time. However, most research has focused on the test data in die level or wafer level. The yield prediction that uses a markov chain is performed by calculating the probability that a chip is acceptable given n defects [3]. However, this prediction is limited due to the univariate analysis on which it is based. Also, multiple discriminant analysis is conducted for multivariate data analysis. However, this method of analysis is limited by the assumption that variables are independent, identical and normally distributed. For the further multivariate analysis, the hybrid machine learning methods are applied in the semiconductor manufacturing domain, using decision tree, artificial neural network, and a self-organizing map (SOM) [4]. Also, the yield prediction is conducted using a fuzzy-based

neural network from the multivariate parametric test data [5]. However, this prior research has focused on the yield in wafer test process. To predict the yield in final test, a stepwise support vector machine (S-SVM) algorithm is applied to the wafer test data [1]. S-SVM classifies the low and high yield of the final test by screening for potential defects in the final test process. As a research about pattern recognition, the study is conducted using wafer clustering and Bayesian inference [7]. Also, self-localization through pattern recognition of wafer using geometric hashing has performed [6]. However, above two studies only focuses on wafer image. Therefore, this study proposes the procedures of selecting features using die level data to more accurately analyze the causes affect failure in final test. As shown in Fig. 2, this study consists of the three steps.

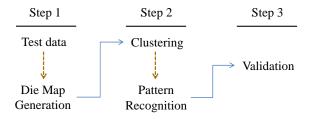


Fig. 2 The proposed 3 steps in this study

In step 1, die-maps are generated from the test data. Die maps represents input variable with regard to clustering. In step 2, feature that reflects the state of dies is selected through clustering. In step 3, we have validated the superiority of selected feature from die-maps.

The rest of this paper is organized as follows. Section II and Section III introduce die-map generation process and clustering analysis for pattern recognition, respectively. Section IV describes the validation concept with regard to the proposed algorithm based on Sections II and III. In Section V, the experimental results are explained after the proposed algorithm is applied to actual industrial data. Finally, a conclusion and further studies are described in Section VI.

II. DIE-MAP GENERATION

This section describes die-map generation process from the test data. The test data consists of the FBC (Fail Bit Count) about each repair area in die. The FBC means the number of failure cells whose repair is required. Also, repair area means minimum unit that can replace fail cells with normal cells at once. Repair is conducted by using spare column or row cells. Using the test data, die-maps were generated in following three types.

- Type A (Column FBC): Colum FBC represents the number of spare column cell that is substituted for repair. As column repair area is greater than the hundreds, repair areas were summarized in a 4 × 4 grid. In other word, die data that contains hundreds of variables are converted to a 4 × 4 die-map.
- **Type B** (Column and row FBC): Type B concurrently considers the number of spare column and row cell that is

- substituted for repair. Like Type A, column and row repair areas were summarized in a 8×1 matrix. The column size of matrix is 1 because the size of column and row area is different each other.
- Type C (Detailed column and row FBC): Type C closely considers the number of spare column and row cell that is substituted for repair. This type is the row area is sliced to be equal to column area. The size of this die-map is 8×8 and this map is expected to include more detailed information.

Fig. 3 represents die-map with regard to Type A. The legend on the right side means the minimum and maximum values of FBC on the wafer and density between two values. Also, 16 features are generated and features mean contrast of each position on the die-map.

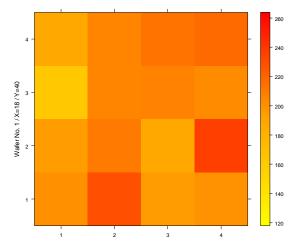


Fig. 3 A 4 by 4 die-map through Type A

Fig. 4 describes die-map with regard to Type B. As the sum of column FBC in repair area with row was used, contrast of each row is uniform. Therefore, in case of Type B, 8 features are generated.

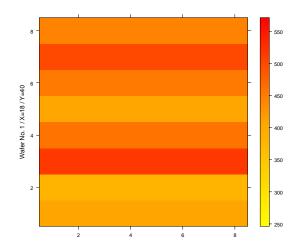


Fig. 4 A 8 by 1 die-map through Type B

Fig. 5 describes die-map with regard to Type C. In case of Type C, as the sum by section (section=8) of column FBC in

repair area with row was used, 64 features are generated.

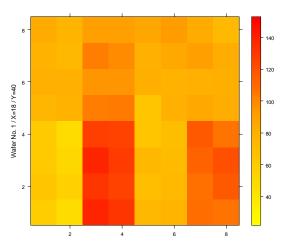


Fig. 5 A 8 by 8 die-map through Type C

III. PATTERN RECOGNITION USING CLUSTERING

This section describes pattern recognition through die-map clustering. In this study, K-means clus11tering is used since K-means clustering is widely known as one of the simplest unsupervised learning algorithms [6].

A. K-Means Clustering

The primary concept of K-means clustering is to group given data set through a certain number of clusters (K-clusters). The calculation procedure of the algorithm is as follows.

Step 1.Makes the initial centroid set $[y_1, ..., y_N]$ of K after K vectors from the data set $[x_1, ..., x_N]$ is randomly selected.

Step 2.If data x_n is closest to y_i , x_n is labeled to belong to X_i . After all the data sets is divided into K clusters $\{X_1, ..., X_k\}$.

$$X_i = \{x_n | d(x_n, y_i) \le d(x_n, y_i), j = 1, \dots K\}$$

Step 3. The centroids of new cluster obtained in Step 2 are updated.

Step 4. The sum of distances between data and the nearest cluster centroid is calculated as the total distortion.

$$D = \sum_{n=1}^{N} d(x_n, y_{i(n)}), if x_n \in X_k, i(n) = k$$

Step 5.Step 2-4 are repeated until fixed number of iterations is reached.

B. Pattern Recognition through Die-Map Clustering

Die-map clustering is performed based on feature from die-map. Features are defined by contrast according to location on the map. The basic concept of die-map clustering is to group dies with similar pattern. The procedure of extracting feature is as follows: First, FBC is converted to contrast level on the die and contrast level represents feature that reflects characteristics of the die-map. As shown in Fig. 6, die-maps are clustered

according to similar patterns. Fig. 6 represents the clustering result about Type C die-map. Die-maps belong to cluster 1 have the lower probability of failure and die-maps belong to cluster 2 have the higher probability of failure. Therefore, this study proposes the best feature among Type A, B and C and defective patterns by through die-map clustering. First, we find out feature affects failure using Cluster Specificity (CS). CS means index that represents the percentage of normal and abnormal dies in each cluster. For example, if the percentage of normal and abnormal dies is 1:1, CS is equal to 0. Also, if CS is closer to 1, the percentage of normal and abnormal dies is higher. In other word, CS is a value that reflects the performance of clustering for selecting best one among given features. Subsequently, we propose a pattern that affects failure most using selected feature.

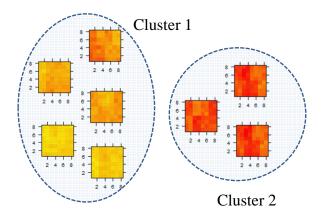


Fig. 6 Clustering result about die-maps from Type C

IV. PROPOSED ALGORITHM

This section describes procedures of proposed algorithm, which consists of four parts in Fig. 7. First, die-map generation is performed to convert amounts of FBC data. Second, the clustering and pattern recognition through features extracted from die-maps are conducted. Finally, we validate the superiority of feature and pattern.

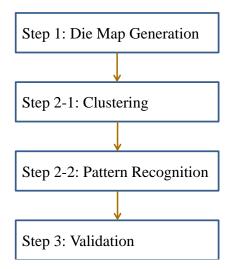


Fig. 7 Overall framework of the proposed algorithm

More detailed description with regards to the proposed algorithm is as in the following.

A. Die Map Generation

As mentioned in Section II, 3 Types die-maps are generated from FBC data set. Each type has a difference with accuracies of density. Type 3 is expected to be better than Type 2. Also, Type 2 is expected to be better feature than Type 2.

B. Clustering and Pattern Recognition

This section describes comparing with 3 features from 3 kinds of die-map and finding out pattern that affects failure. First, clustering is performed using 3 features from 3 die-map data. Subsequently, the best feature is selected by comparing CS value defined in Section III-B. Second, using selected feature, we find out pattern affects failure in final test. For finding out pattern, heuristic algorithm was used.

C. Validation

For evaluating applicability of selected feature, we have compared the performance of three data mining models using 3 types feature. For experiment, Support Vector Machine, Artificial Neural Network and Decision Tree are used.

V.EXPERIMENTAL RESULTS

For the experiment, an actual industrial data set is used. The original data set includes 13 wafers, consisting of approximately 1400 observations.

This experiment consists of two parts. The first is to select more significant feature through die-map clustering. The second experiment evaluates the performance of three data mining model using 3 proposed features in this study. The data mining model considers Support Vector Machine, Neural Network and Decision Tree that are widely used for classification or regression.

To compare the performance of clustering by each Type, CS value is used in Section III-B. The higher CS is the better clustering performance is. Fig. 8 represents CS values according to feature of 3 Types.

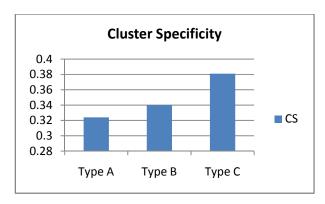


Fig. 8 Comparing with CS values about 3 Types features

64 features from Type C are more significant than other Types in die-map clustering. Therefore, it is desirable that the original FBC data consisting of hundreds of variables is converted to 64 features. For validation about features from

Type C, we have compared the performance of classification algorithms. In general, data set should be separated to training and test set to evaluate the performance of learning algorithm. However, as this study focuses on selecting feature affects failure in final test of semiconductor manufacturing process, the algorithm performance about training set is compared. Table I represents the classification accuracies with regard to 3 classification algorithms.

TABLE I
PERFORMANCE OF 3 CLASSIFICATION MODELS

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Model		Type A	Type B	Type C
Decision Tree	FCA	0.8225	0.7830	0.8354
	PCA	0.7972	0.8069	0.8352
Support Vector Machine	FCA	0.8635	0.6084	0.9489
	PCA	0.8795	0.6934	0.9619
Artificial Neural Network	FCA	0.4382	0.7478	0.9461
	PCA	0.7391	0.3785	0.2885

To evaluate the performance of the algorithms, we compared the FCA (Fail Classification Accuracy) and PCA (Pass Classification Accuracy). FCA means the percentage whose observations classified as Fail class is regarded as actual Fail class. PCA means the percentage whose observations classified as Pass class are regarded as actual Pass class. Except for PCA of Neural Network, 64 features from Type C are significant in all cases. Because Artificial Neural Network algorithm is sensitive in selecting model parameters, learning performance is not uniform.

VI. CONCLUSION

As the semiconductor test process consists of many test stages and each stage generates a large amount of test data, big data analysis is essential. Therefore, this study proposes the procedures of feature extraction from FBC data consisting of hundreds of variables. Also, this proposed procedure is applied to real industrial data and its applicability is verified. For the further study, the performance of classification algorithms is evaluated about both training and test set. Also, many more data sets need to be applied to this proposed algorithm to test the robustness of these results.

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REFERENCES

[1] An, D., Ko, H.H., Gulambar, T., Kim, J., Baek, J.G., and Kim, S., "A Semiconductor Yields Prediction Using Stepwise Support Vector Machine", IEEE International Symposium on Assembly and Manufacturing, December 2009.

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- [2] Uzsoy, R., C. Lee, and L.A. Martin-Vega, "A Review of Production Planning and Scheduling models in the Semiconductor Industry PART I: System Characteristics, Performance Evaluation and Production Planning." IIE Transactions, Vol. 24, No. 4, pp. 47-60, 1992.
- System Characteristics, Performance Evaluation and Production Planning," IIE Transactions, Vol. 24, No. 4, pp. 47-60, 1992.

 [3] Ciciani, B. and G. Jazeolla, "A Markov Chain-Based Yield Formula for VLSI Fault-Tolerant Chips," IEEE Transactions on Computer-Aided Design, Vol. 10, No.2, pp. 252-259, 1991.
- 4] Kang, B.S., Lee, L.H., Shin, C.K., Yu, S.L., & Park, S.C., "Hybrid machine learning system for integrated yield management in semiconductor manufacturing," Expert Systems with Applications, Vol. 15, No. 2, pp. 123-132, August 1998.
- [5] Wu, L., and Zhang, J., "Fuzzy neural network based yield prediction model for semiconductor manufacturing system", International Journal of Production Research, Vol. 48, No. 11, pp. 3225-3243, June 2010.
- [6] Jyoti, K., and Singh, S., "Data Clustering Approach to Industrial Process Monitoring, Fault Detection and Isolation", International Journal of Computer Applications, Vol.17, No. 2, Article8, March 2011.
- [7] Tao, Y., and Way, K., "Spatial defect pattern recognition on semiconductor wafers using model-based clustering and Bayesian inference", European Journal of Operation Research, Vol. 190, No 1, pp. 228-240, October 2008.

Seung Hwan Park received his B.S. degree in Computer Science and M.S. degree in Industrial Management Engineering from Korea University, Korea.

He was a programming researcher at Tmax Soft from 2008 to 2009. He is currently a Ph.D. candidate in Industrial Management Engineering. His research interests are in statistical analysis and data-mining algorithms and application

Cheong-Sool Park is a Ph.D. candidate in Industrial Engineering at Korea University. He holds B.S. and M.S. degrees in Industrial Engineering from Korea University.

From 2005 to 2006, he worked as a research analyst at Samsung Economic Research Institute. In 2007, he worked as a researcher at the Institute for Advanced Engineering. His research is primarily in the field of data mining for manufacturing systems. He has a particular interest in modeling and analyzing time effects.

Jun Seok Kim is a postdoctoral research fellow at the School of Industrial Management Engineering at Korea University. He holds B.S. and M.S. degrees in Industrial Systems and Information Engineering and a Ph.D. in Information Management Engineering from Korea University. His research interests include statistical process control and data-mining algorithms.

Youngji Yoo received her B.S. degree in Information Statistics and Industrial Management Engineering from Korea University, Korea.

She is currently in an integrated master and doctor degree course. Her research interests are in statistical analysis and application of data mining in production system.

Daewoong An received his B.S. degree in Electronic Engineering and M.S. degree in Industrial Management Engineering from Korea University, Korea.

He has been working as a product analysis engineer especially DRAM product at SK Hynix from 2000. His research interests are in statistical analysis, data mining and big data analysis.

Jun-Geol Baek received B.S., M.S., and Ph.D. degrees in Industrial Engineering from Korea University in 1993, 1995, and 2001, respectively.

From 2002 to 2007, he was an assistant professor in the Department of Industrial Systems Engineering at Induk Institute of Technology, Seoul, Korea. He was also an assistant professor in the Department of Business Administration at Kwangwoon University, Seoul, Korea, from 2007 to 2008. In 2008, he joined the School of Industrial Management Engineering at Korea University, where he is now a professor. His research interests include statistical process control, fault detection and classification, advanced process control, and applications of data mining in production systems.