Design of Low Power and High Speed Digital IIR Filter in 45nm with Optimized CSA for Digital Signal Processing Applications

G. Ramana Murthy, C. Senthilpari, P. Velrajkumar, Lim Tien Sze

Abstract—In this paper, a design methodology to implement low-power and high-speed 2nd order recursive digital Infinite Impulse Response (IIR) filter has been proposed. Since IIR filters suffer from a large number of constant multiplications, the proposed method replaces the constant multiplications by using addition/subtraction and shift operations. The proposed new 6T adder cell is used as the Carry-Save Adder (CSA) to implement addition/subtraction operations in the design of recursive section IIR filter to reduce the propagation delay. Furthermore, high-level algorithms designed for the optimization of the number of CSA blocks are used to reduce the complexity of the IIR filter. The DSCH3 tool is used to generate the schematic of the proposed 6T CSA based shift-adds architecture design and it is analyzed by using Microwind CAD tool to synthesize low-complexity and high-speed IIR filters. The proposed design outperforms in terms of power, propagation delay, area and throughput when compared with MUX-12T, MCIT-7T based CSA adder filter design. It is observed from the experimental results that the proposed 6T based design method can find better IIR filter designs in terms of power and delay than those obtained by using efficient general multipliers.

Keywords—CSA Full Adder, Delay unit, IIR filter, Low-Power, PDP, Parametric Analysis, Propagation Delay, Throughput, VLSI.

I. INTRODUCTION

DIGITAL filtering is one of the most widely used operations in digital signal and image processing applications. The purpose of the filtering operation is to transform the input signal or image in such a way to enhance or suppress certain features. There are two types of digital filters that are used in digital signal and image processing, namely the finite impulse response (FIR) and the infinite impulse response (IIR). High speed VLSI implementation of both of these filtering approaches is of great interest in digital signal processing. IIR digital filters compute their outputs recursively, i.e., they need the immediate past output for computing the current one. Thus IIR digital filters are more difficult to pipeline than FIR filters.

On the other hand, the IIR digital filters have the advantages of high selectivity and requiring fewer coefficients than the FIR digital filters with similar performance. Consequently, realization of IIR digital filters with good overall performance became a challenging aspect to many authors. Systolic arrays are architectures which respond to the requirements of VLSI design by their simplicity, modularity and nearest neighbor connectivity. These characteristics give the systolic arrays a leading edge over other VLSI architectures. Several systolic array designs to compute the IIR digital filtering operation have been proposed [1], [2]. Most methods proposed for such a systolic realization are based on the bit-parallel structures. The absence of inherent delay elements inside the feedback loop has limited the possibility of pipelining and consequently the throughput rate of the existing fully bit parallel systolic IIR digital filter architectures. The minimum achievable time cycle for the conventional implementations of systolic IIR digital filters is that of one bit-parallel multiplication plus that of two bit-parallel additions.

One way to achieve pipelining of IIR digital filters is to insert delay elements in the feedback loop. This can be achieved by using the scattered look ahead technique [3], [4] or the clustered look ahead technique [5], [6]. The application of the scattered look ahead computation technique has showed that by iterating the algorithm to the level of pipelining required, high throughput rate can be achieved. Although it guarantees stability, the drawback of this scheme is the overhead in hardware complexity which is proportional to the number of pipelining levels. The clustered look ahead technique at first seems quite superior by requires less overhead. However, the stability of the filter is not assured. Although, the generalized clustered look ahead proposed in [5] guaranties stability, it still requires 20% increase in hardware complexity for two levels of pipelining. The proposed design uses carry save adder technique along with the delay elements to implement the pipelined IIR digital filter. The proposed 6T adder cell used as CSA in the design makes it less complex, high speed and better throughput when compared with similar designs.

The rest of the paper is organized as follows. Section II briefly describes the review of IIR digital filter structures reported in the literature. Proposed 6T CSA based IIR filter is described in Section III. Section IV presents the simulation results and comparison with the recently published author's. Power dissipation versus capacitance, input voltage, temperature and Monte-Carlo in parametric analysis results

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are shown in Section V and conclusions are drawn in Section VI.

II. REVIEW OF IIR DIGITAL FILTER STRUCTURES

IIR digital filters are recursive systems that involve fewer design parameters, less memory requirements and lower computational complexity than finite impulse response (FIR) digital filters. These are the primary advantages of implementing IIR digital filters. If there is no requirement for a linear-phase characteristic within the pass-band of a digital filter, the aforementioned advantages make IIR filters more attractive to a system designer [7]. This type of recursive system belongs to an important class of linear time-invariant discrete-time systems characterized by the general linear constant-coefficient difference equation as shown in (1).

$$y(n) = -\sum_{k=1}^{N} a_k y(n-k) + \sum_{k=0}^{M} b_k x(n-k) \qquad (1)$$

Transforming this difference equation into the z-domain by means of the z-transform, such a class of linear time-invariant discrete-time systems is also characterized by the transfer function as shown in (2).

$$H(z) = \frac{\sum_{k=0}^{M} b_k z^{-k}}{1 + \sum_{k=1}^{N} a_k z^{-k}} \qquad (2)$$

Different structures of IIR filters are described by the difference equation in (1). These structures are referred to as direct-form realizations. It should be noted that although these structures are different from one another by design, they are all functionally equivalent. Three prominent direct-form realizations are the Direct-Form I, the Direct-Form II and the Transposed Direct-Form II structures. In terms of hardware implementation, the Direct-Form I structure requires M+ N+ 1 multiplication, M+N additions, and M+N+1 memory locations. Fig. 1 (a) depicts this structure as implemented from (2).
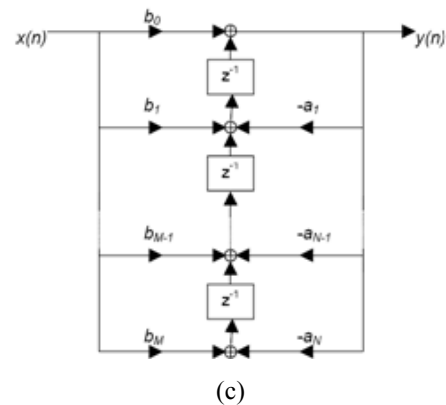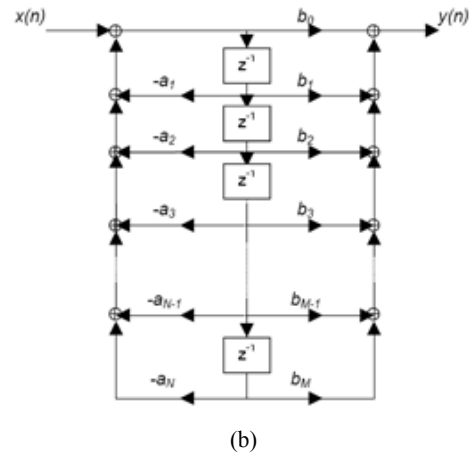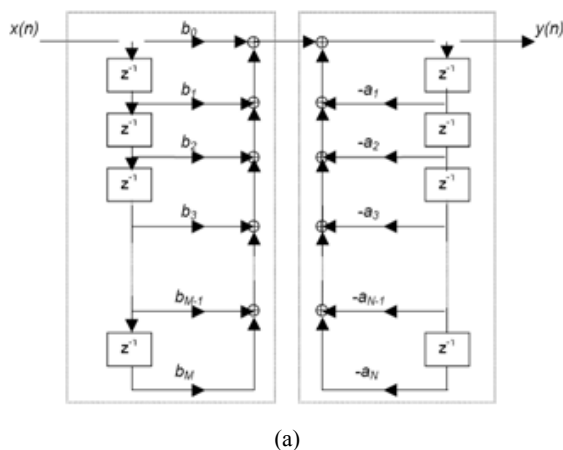

(a)

(b)

(c)

Fig. 1 (a) Direct-Form I Realization (b) Direct-Form II Realization
(c) Transposed Direct-Form II Structure

The Direct-Form II structures require M+N+1 multiplications, M+N additions, and the maximum of {M,N} memory locations. Because the Direct-Form II structure requires less memory locations than the Direct- Form I structure, it is referred to as being canonic. Fig. 1 (b) shows an IIR digital filter in Direct-Form II format.

Mathematical manipulation of (1) based on Fig. 1 (b) yields the Transposed Direct-Form II structure. This structure requires the same number of multiplications, additions, and memory locations as the original Direct-Form II structure. Both Direct-Form II structures are more design-preferable compared to the Direct-Form I structure. This is because of the smaller number of memory locations required in their implementation. Fig. 1 (c) shows an example of the Transposed Direct-Form II structure. Because of this fact, for hardware considerations the Transposed Direct-Form II structure is the structure of choice for designing quantized, fixed-point IIR digital filters and its transfer function is as shown in (3).

$$H(z) = \frac{b_0 + b_1 Z^{-1} + ... + b_{M-1} Z^{M-1} + b_M Z^M}{1 + a_1 Z^{-1} + ... + a_{N-1} Z^{N-1} + a_N Z^{-N}} \qquad (3)$$

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A. Hardware Considerations

Due to finite-precision arithmetic in the realization of n-bit quantized digital filters, nonlinear effects make it extremely difficult to both analyze precisely and predict with 100% accuracy filter performance. Fixed-point realization of digital filters makes quantization effects very important. Nonlinear effects at the filter output become a greater problem with high-order filters; the solution to significantly minimize nonlinear effects is to decompose digital filters with orders greater than 2 into 2nd order sub-blocks. There are two methods in which decomposing high-order digital filters into 2nd order sub-blocks can achieve the goal of minimization of nonlinear effects. These methods are the parallel-form structure and cascade-form structure.

B. Parallel-Form Structure

Parallel-form realization of an IIR digital filter can be obtained by performing a partial-fraction expansion on the transfer function H(z). Performing this mathematical function produces the resulting transfer function in the form as shown in (4).

$$H(z) = C + \sum_{k=1}^{K} H_k(z) \qquad (4)$$

The function $H_k(z)$ is in 2nd order form as shown in (5)

$$H_k(z) = \frac{b_{k0} + b_{k1}z^{-1}}{1 + a_{k1}z^{-1} + a_{k2}z^{-2}} \qquad (5)$$

It should be noted that the transfer functions in (4) and (2) are functionally equivalent in that both are ideal representations of an infinite-precision filter. In (4), the constant K is defined as the integer part of (N+1)/2. The constant N is the same constant N in (1). Transfer function H(z) is generally composed of poles and coefficients (residues) of the partial-fraction expansion. A more direct result of the partial-fraction expansion of H(z) in (2) yields the functional equivalent as shown in (6).

$$H(z) = C + \sum_{k=1}^{N} \frac{A_k}{1 - p_k z^{-1}} \qquad (6)$$

The variables p_k and A_k stand for the poles and residues, respectively, in the partial-fraction expansion. The constant C is the same as the variable used in (4). If N is odd then C = 0. If N is even then C = bN/aN. Fig. 4 (a) graphically illustrates a parallel-form structure of an IIR digital filter. The Transposed Direct-Form II realization of each 2nd order sub-block is illustrated in Fig. 4 (b) [7].
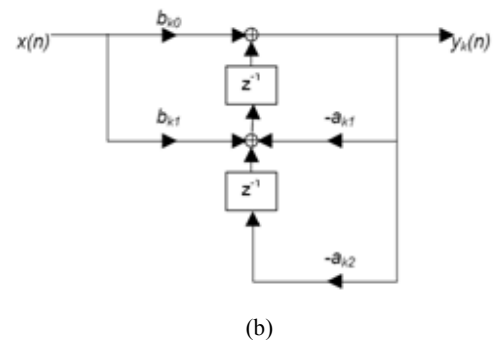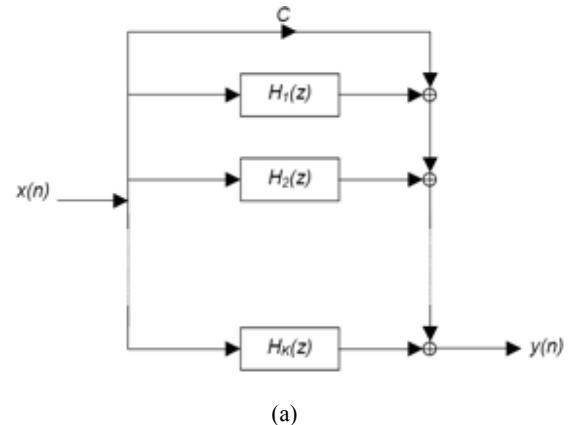

(a)

(b)

Fig. 2 (a) Parallel-Form IIR filter (b) 2nd order section of parallel-form

C. Carry-Save Adder

A carry save adder (CSA) tree consists of CSA operators and one adder at the root of the tree. The CSA operators are used to transform an arbitrary number of operands in the addition process to produce two adding operands, after which the adder at the root of the CSA tree computes the final sum. The proposed design uses this technique to implement the adder/subtraction section along with the delay elements in the pipelining recursive section of the digital IIR filter.

The 1-bit multi-operand addition can be extended to the n-bit multi-operand addition by cascading the CSA operators. An n-bit CSA consists of n disjoint FAs operating in parallel. Each FA has three i [th] bit inputs and generates two outputs namely an i [th] bit partial sum, S and an i [th] bit carry, C. As for adding more than three operands, there is a second or further subsequent levels of the CSA operators. They receive the S and C from the previous CSA operator level, together with another input operand, and produce a set of new S and C values. The implementation of CSA can be further expanded to add k operands. In this case (k − 2) CSA levels and one CPA are required to realize the addition operation [8]. The time to obtain the summation is as shown in (7).

$$T = (k-2) \times T_{CSA} + T_{CPA} \qquad (7)$$

III. DESIGN METHOD

IIR filters can be implemented using a 'hardwired' architecture suited to high performance, or a more traditional

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approach based on general multiply-accumulate units. In case of IIR filters, however, the hardwired implementation is significantly more desirable than the alternate approach due to the difficulty in rescheduling multiplexed processing elements in a system with feedback. An architecture that is reconfigured to implement different filters will generally provide both high performance and good area efficiency. A traditional approach to the realization of IIR filters using multiply-accumulate units is also possible, but may be less efficient. The general architecture is filter with slight modifications to the routing between arithmetic units and support for scaling necessary in an IIR biquad section [9].

It is well known that the fastest FIR filters have been implemented by using both carry-save arithmetic and filter coefficients represented efficiently as hard-wired power-of-two digits. Therefore it might be expected that similar design techniques will be useful in this attempt to enable pipelined IIR filters to operate at speeds comparable to their FIR counterparts [10]. The filter implementation strategy is as shown in Fig. 3. The use of carry save adder (CSA) arithmetic pipelining not only speeds up the data rate but also allow the multiplier precision to be increased. By using carry-save arithmetic, all additions with carry propagation can be moved out of a filter's recursive loop. The proposed 6T adder cell is used as the full adder carry save arithmetic block. In this way a fast second-order IIR filter (recursive portion) can be implemented as shown in Fig. 3. Notice that all adders in the feedback loop are carry-save adders. (Thus they- have three inputs and two outputs.) Furthermore, one fast pipelined half adder is located outside the loop. High-speed multipliers are usually implemented by carry-save adder arrays, and now the number of such arrays is doubled to four. Thus, a complete second-order IIR filter section, including the non-recursive part, needs six or seven multipliers, depending on how the scaling operation is performed. In case each multiplier coefficient is approximated by three power-of-two digits (which is roughly equivalent to a 10-bit signed binary number) the carry-save adders configured in a tree-structure can be used to implement this second-order filter section.

A. Delay Unit

A master slave D flip – flop circuit is designed by using complementary pass transistor logic as a delay unit in this design. These delay units don't use the external clock input as it introduces the additional delay in the recursive portion of the filter and is always assumed to be high.

IV. RESULTS AND DISCUSSION

The three different CSA circuits such as MUX-12T [14], MCIT-7T [15] and the proposed 6T [16] are used as full adder blocks in the feedback loop of the pipelined IIR filter recursive section along with the proposed pass- transistor logic delay units are schematized by using DSCH3 CAD tool. The proposed full adder based IIR filter and other two adder based IIR filter layouts are analyzed in 45nm feature size by using Microwind 3. The CSA circuit performance depends on the transistor count as well as design concept. The MCIT-7T CSA

circuit is designed by multiplexing control input technique. The transient of input nodes consume more power which leads to high power consumption in the circuit. The MUX-12T CSA circuit is designed by multiplexing control input technique. The carry circuit has buffering restoration unit at and its complement leads to high power dissipation and propagation delay. The proposed 6T adder based IIR filter gives less power dissipation, propagation delay, less occupying area and high throughput compared to other two existing adder based IIR filter circuits as shown in Table I. The multiplexing design concept used in the proposed 6T CSA cell reduces leakage current due to less transistor count and switching event in the transistors.

The proposed 6T CSA based IIR filter is also compared with few recently published authors' IIR filters at various feature sizes as shown in Table II. Compared with Ravinder et al. [11], the proposed 6T IIR filter gives 95.61 %, 93.55% reduction in propagation delay for Spartan 3E, Virtex 2P respectively due to the presence of floating mask concept for supply voltage in adder circuits. The power dissipation in the proposed 6T CSA IIR filter is reduced due to highly tasked flow of current and the absence of swing restoration. It gives 99.71% less power dissipation, 98.04% lower delay for MUL & REG and 99.68% less power dissipation, 97.06% lower delay for MUL & AND gates when compared with Dutta et al. [12] due to high critical path for sum and carry as the number of logic gates is high in the design. The proposed 6T CSA IIR filter when compared with Deepa et al. [13] gives 99.99% reduction in power, 14.59% reduction in propagation delay for Kogge Stone due to the calculation of carries corresponding to every bit with the help of group generate and group propagate, 99.99% reduction in power, 74.32% reduction in delay for Sklonsky due to the expense of fan-outs that doubles at each level, 11.53% reduction in power, 71.69% reduction in delay for Brentkung due to the computation of prefixes for 2-bit groups for each input, 99.99% reduction in power, 99.66% reduction in delay for Hancarlson due to the expense of fan-outs and computation of prefixes and 17.26% reduction in power, 3.01% more delay for Ling adder based filter designs. The proposed 6T adder gives more delay compared to the Ling adder based design due to the simplification of carry computation involved at each level. The better performance of the proposed 6T IIR filter is mainly due to highly tasked flow of current, absence of swing restoration, less transistor count, high transition activity in NMOS transistors and low critical path in the CSA circuit used in the design as well as the efficient CPL delay unit implementation.

V. PARAMETRIC ANALYSIS

The layout parameters are calculated from total transistors of the circuit, wires and input/output pads. Power in modern digital CMOS integrated circuits has traditionally been dominated by dynamic switching power. However, as technology scale leakage currents become increasingly large and must be taken into account to minimize total power consumption [17]. Once the magnitude and general shape of the curve has been examined, the measurements can be done

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using a linear scale for current. The proposed 6T IIR filter is compared with the other two filters in parametric analysis such as capacitance versus power dissipation, voltage versus power dissipation, temperature versus power dissipation and Monte-Carlo versus power dissipation by using BSIM 4. The circuit layout capacitance versus power dissipation of the filter circuits are shown in Fig. 4 (a). From the layout dimensions of

filter circuits the capacitance C_{Dn} at the output node can be found as shown in (8).

$$C_{Dn} = C_{GSn} + C_{DBn} = \frac{1}{2}C_{xx}L'W_n + C_{jn}A_n + C_{jswn}P_n \qquad (8)$$
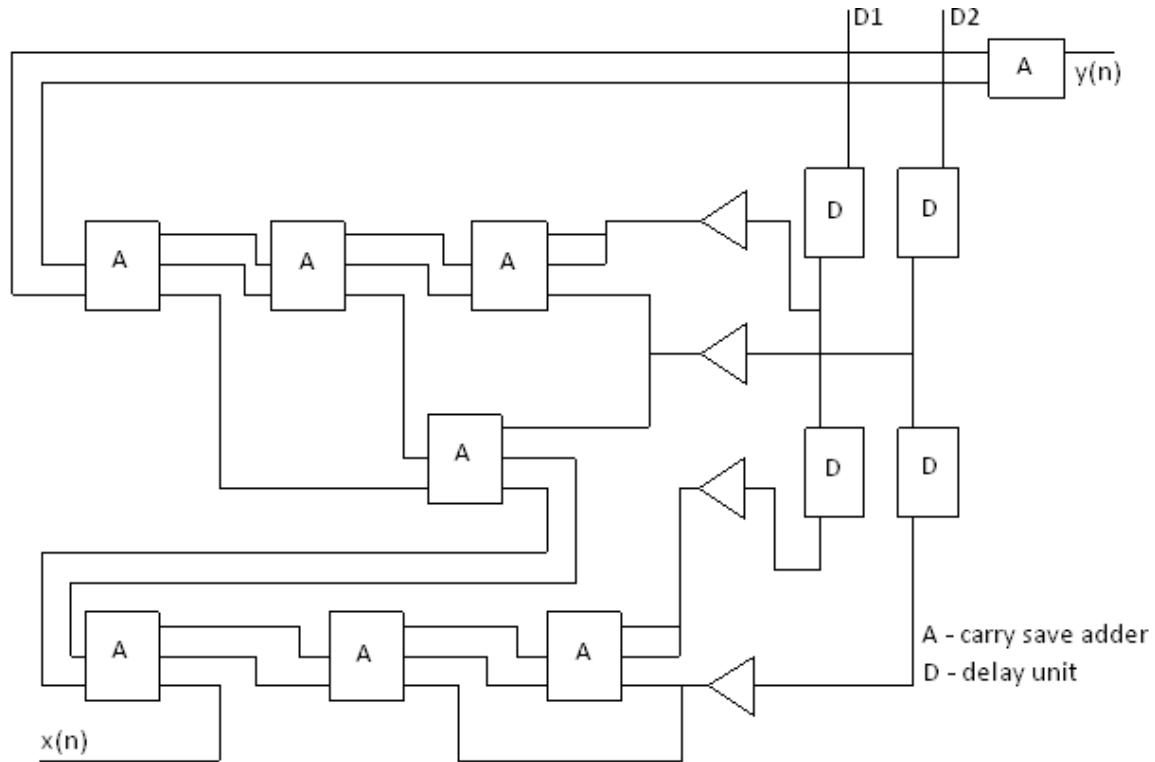
Fig. 3 Implementation of a second order IIR filter using carry-save arithmetic

TABLE I
GATE LEVEL DESIGN FOR IIR FILTERS USING CARRY SELECT ADDERS CELLS FOR POWER DISSIPATION, PROPAGATION DELAY, AREA AND THROUGHPUT

Filter type	Supply Voltage	45nm	65nm	90nm	130nm	180nm	0.25μm	0.35μm
This work (Proposed filter)	Power (μW)	0.115	1.003	1.736	9.531	1086.04	5285.44	9664.33
	Delay (ns)	0.199	0.146	0.846	1.893	2.332	2.809	7.832
	Area (μm²)	131 x 16	110x11	142 x 18	197 x 21	309 x 42	512 x 52	818 x 84
	Throughput (G bit/sec)	2.227	2.525	0.912	0.466	0.387	0.326	0.123
MUX-12T	Power (μW)	0.166	2.897	2.882	10.816	1606.81	5356.51	15139.16
	Delay (ns)	0.461	0.522	1.228	2.971	3.807	4.011	10.352
	Area (μm²)	157 x 18	116 x 12	164 x 19	215 x 23	405 x 45	538 x 52	860 x 84
	Throughput (G bit/sec)	1.406	1.295	0.676	0.310	0.246	0.234	0.094
MCIT-7T	Power (μW)	0.237	3.314	3.318	12.798	1614.04	5680.69	16112.73
	Delay (ns)	0.792	0.871	2.391	3.725	4.191	4.884	12.725
	Area (μm²)	166 x 16	118 x 12	172 x 18	207 x 21	430 x 42	621 x 51	910 x 87
	Throughput (G bit/sec)	0.959	0.892	0.378	0.251	0.225	0.194	0.077
MUX-14T	Power (μW)	0.352	6.071	4.312	18.161	1661.08	6135.21	17231.66
	Delay (ns)	0.979	1.363	3.046	4.703	5.332	6.589	14.198
	Area (μm²)	233 x 15	166 x 10	242 x 16	291 x 20	605 x 39	757 x 49	1210 x 91
	Throughput (G bit/sec)	0.813	0.619	0.303	0.201	0.179	0.146	0.069
Shannon	Power (μW)	0.366	6.102	4.657	19.531	2654.88	7495.24	17970.91
	Delay (ns)	1.841	1.572	3.594	4.934	5.953	7.691	17.326
	Area (μm²)	233 x 17	166 x 12	242 x 19	291 x 23	605 x 46	757 x 57	1210 x 93
	Throughput (G bit/sec)	0.478	0.548	0.260	0.192	0.161	0.125	0.056

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TABLE II
COMPARISON OF THE PROPOSED 6T CSA IIR FILTER FOR POWER
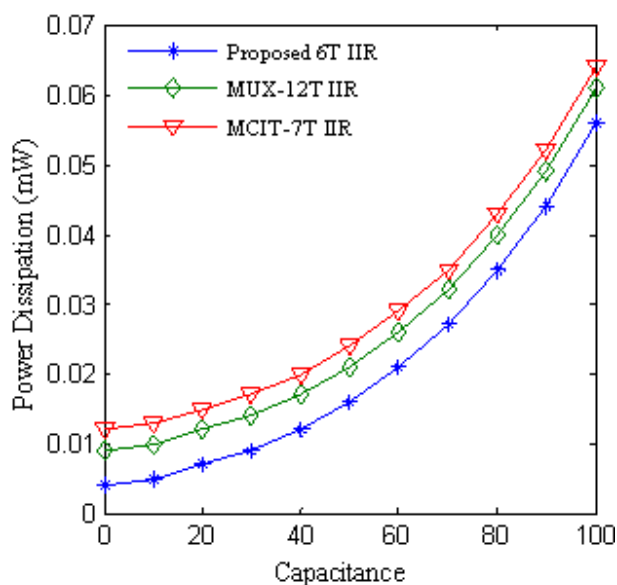DISSIPATION, AND PROPAGATION DELAY WITH THE OTHER PUBLISHED
AUTHORS

Reference	Power (μW)	Delay (nS)
Proposed 6T IIR	0.115	0.199
Ravinder [11] Spartan 3E	-	4.534
Virtex 2P	-	3.09
Dutta [12] MUL & Reg	40	10.178
MUL & AND gates	36	6.788
Deepa [13] Kogge Stone	1879	0.233
Sklonsky	8920	0.775
BrentKung	0.13	0.703
Hancarlson	1917.8	60.18
Ling	0.139	0.193

In the filter circuit it is significant to remember that increasing the channel width of a FET increases the parasitic capacitance values. The total output capacitance calculated by using the switching times of the transistor is used to drive an external load capacitance CL. Thus the total output capacitance of the filter circuit can be calculated as shown in (9).
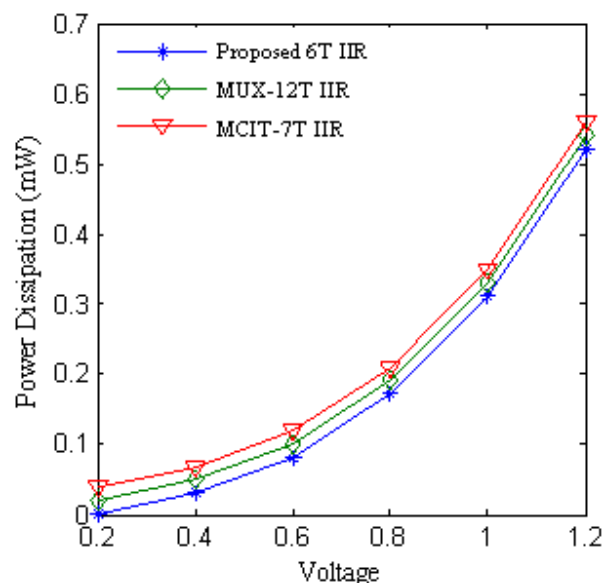
$$C_{out} = C_{FET} + C_L \qquad (9)$$

According to parametric analysis it is evident that the parasitic internal contributions cannot be eliminated. These add with CL since all elements are in parallel. The total output capacitance C_{out} is the load that the gate must drive and the numerical value varies with the load. The charging level of the FET can be calculated as shown in (10).
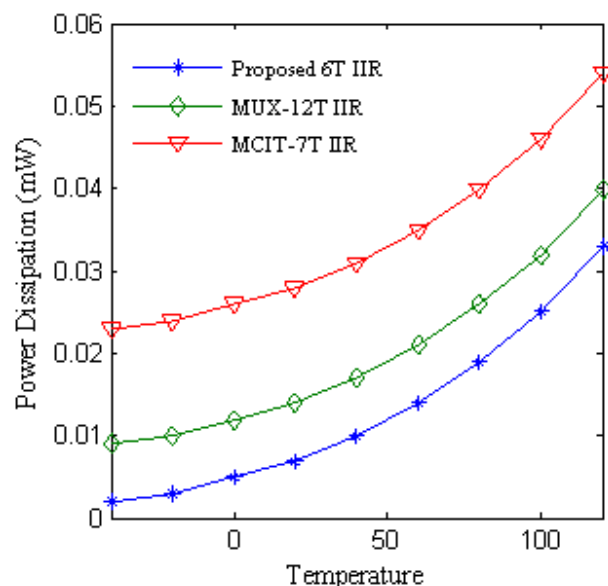
$$Q_e = C_{out}V_{DD} \qquad (10)$$

(b)

(c)

(a)

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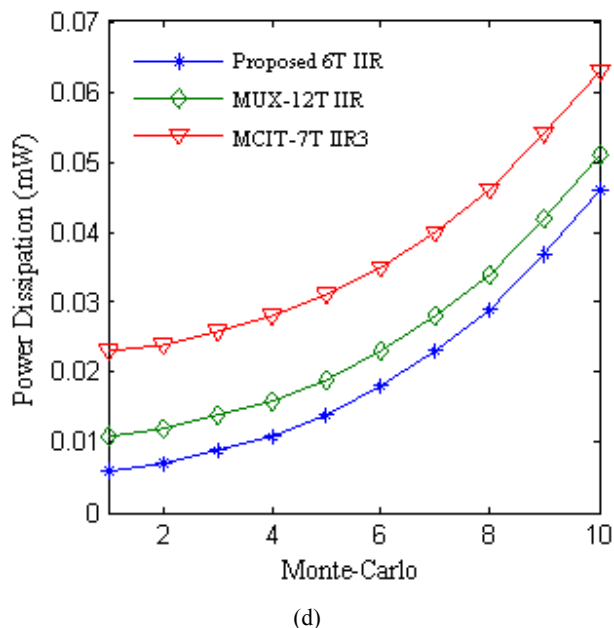International Journal of Electrical and Computer Engineering
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(d)

Fig. 4 (a) Capacitance Vs Power dissipation for the proposed filter (b) Input Voltage Vs Power dissipation for the proposed filter (c) Temperature Vs Power dissipation for the proposed filter (d) Monte-Carlo Vs Power dissipation for the proposed filter

The total output dynamic power dissipation of the filter circuit can be calculated by the sum of average power and short circuit power as shown in (11) over a single cycle with a period of T.

$$P = V_{DD}I_{DDQ} + C_{out}V_{DD}^2 f \qquad (11)$$

The dynamic power dissipation in the filter circuit is directly proportional to the signal frequency. The proposed 6T IIR filter gives lower power dissipation than MUX-12T IIR and MCIT-7T IIR circuits. The load capacitance (C_L) represents the power dissipated during a switching event. The output node voltage makes a power transition, when load capacitance values are increased irrespectively of supply voltage level. Generally, in digital CMOS circuit's dynamic power is dissipated when energy is drawn from the power supply voltage to charge up, which is clearly identified in Fig. 4 (b).

The circuit layout temperature versus power dissipation of the proposed 6T IIR filter adder along with the two other IIR filters is shown in Fig. 4 (c). The temperature analysis depends upon the layout junction temperature (T_j) case temperature (T_{cj}) and its coefficient (Θ_{ij}). The power dissipation of the adder layout is shown in (12).

$$P_D = \frac{T_j - T_{cj}}{\theta_{ij}} \qquad (12)$$

When θ_{ij} is constant the power dissipation is directly proportional to junction temperature. The proposed 6T IIR filter gives lower power dissipation when compared to the

other two filters in terms of varying temperature due to the regular arrangement of MUX circuits as well as the absence of layout gap in the design of the CSA adder cell.

Monte Carlo simulation can be used to find the effects of random variations in a circuit. It consists of running a simulation repeatedly with different randomly chosen parameter off-sets.

The transistor models must include the offset parameters while using Monte Carlo simulation. Power dissipation in the pass transistor logic is moderately high due to the presence of dynamic power dissipation in NMOS transistors. In the proposed 6-T IIR filter circuit switching characteristics are balanced so the current flow of the carriers is regulated. The gate capacitance is also important for dynamic power consumption, as shown in (13).

$$P_{dynamic} = \frac{V_{DD}}{T}[Tf_{sw}CV_{DD}] = CV_{DD}^2 f_{sw} \qquad (13)$$

The effective gate capacitance for power is typically somewhat higher than for delay because Cgd is effectively doubled from the Miller effect due to the delay in the drain to completely switch. Power dissipation of the proposed 6-T adder circuit and the other two filter circuits in Monte Carlo simulation is as shown in Fig. 4 (d) clearly indicate that the proposed filter design performance is better compared with the other two filter circuits. The effective capacitance for dynamic power consumption is as shown in (14).

$$C_{eff-power} = \frac{\int i_{in}(t)dt}{V_{DD}} \qquad (14)$$

where this capacitance can be divided by the total transistor width to find the effective capacitance per micron. The proposed 6T IIR is designed with the regular arrangement of transistors and low critical path leads to low power dissipation compared with the other filter circuits.

VI. CONCLUSION

In this paper a new 6T CSA transformation, a method for designing efficient stable pipelined IIR filters has been proposed. The proposed filter along with MUX-12T, MCIT-7T CSA based IIR filters are designed by using DSCH 3 and layouts are generated by using Microwind 3 CAD tool. The comparison has been carried out in terms of power, propagation delay, PDP and throughput for circuit optimization. The parametric analysis is done by using BSIM 4 tool. The power dissipation comparison of the proposed IIR filter is done for load capacitance, input voltage, temperature and Monte-Carlo and the results show better performance than the other two IIR filter circuits. Thus the proposed 6T CSA IIR filter may be suitable at low voltage, high speed digital signal processing as well as image processing applications.

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