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Leakage Reduction ONOFIC Approach for Deep Submicron VLSI Circuits Design

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***Abstract*—**Minimizations of power dissipation, chip area with higher circuit performance are the necessary and key parameters in deep submicron regime. The leakage current increases sharply in deep submicron regime and directly affected the power dissipation of the logic circuits. In deep submicron region the power dissipation as well as high performance is the crucial concern since increasing importance of portable systems. Number of leakage reduction techniques employed to reduce the leakage current in deep submicron region but they have some trade-off to control the leakage current. ONOFIC approach gives an excellent agreement between power dissipation and propagation delay for designing the efficient CMOS logic circuits. In this article ONOFIC approach is compared with LECTOR technique and output results show that ONOFIC approach significantly reduces the power dissipation and enhance the speed of the logic circuits. The lower power delay product is the big outcome of this approach and makes it an influential leakage reduction technique.

***Keywords*—**Deep submicron, Leakage Current, LECTOR, ONOFIC, Power Delay Product.

I. Introduction

LOW power circuit design is the three dimensional problem involving chip area, power dissipation and performance trade-offs. The trend of shrinking the device dimensions decreases the chip area requirement for the logic circuit implementation in deep submicron region [1], [2]. The supply voltage must be reducing as technology node moves towards deep submicron regime to give the reliability of the logic circuit. Supply voltages play an imperative role to control the power consumption and hence power dissipation in portable electronic devices [3]. Supply voltage scaling without scaling of threshold voltage degrades the performance of the device. For retaining the performance of the device the supply voltage and threshold voltage must be reduced proportionally as the CMOS technology scales down. The reduction in the threshold voltage causes an exponential increase in the leakage current of about five times per generation [4], [5].

Power dissipation of Integrated circuits has been increasing quickly as we move to new lower technology node. Fig. 1 indicates the importance of leakage current with reducing the physical gate length. This plot shows that, leakage power dissipation has been mounting at a noticeably faster rate as technology scaled down [6].

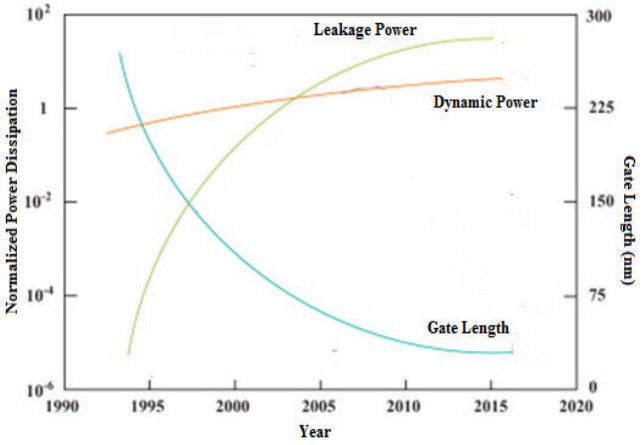

Fig. 1 Recent Power Dissipation Trends

A good VLSI designer always seems for developing an efficient leakage reduction technique to reduce leakage current in deep submicron regime. In this paper, we describe a new leakage reduction technique called On/OFF logIC (ONOFIC) approach for designing low power high performance CMOS circuits. The rest of the paper is organized as follows. Section II concisely explains the prior work on the leakage reduction techniques and their limitations. Section III describes our proposed leakage reduction ONOFIC approach. Results and discussions are presented in Section IV then conclusion in Section V.

II. Related Previous Work

The leakage power dissipation arises in active as well as standby mode of the devices so leakage reduction techniques are widely required for designing the logic circuits in deep submicron regime. In [7], multi-threshold CMOS technique uses the model of virtual power rail. The virtual power/ground line is connected to the actual power/ground through a high threshold sleep transistor. MTCMOS increases chip area and difficulty of auto monitoring sleep signals while this technique is applicable only for standby mode leakage reduction. It required two different threshold voltage transistors that cause additional mask layers are needed. In [8] S. Narendra et al. found out that the leakage power of a logic circuit can be minimized by applying a number of off state transistors in series. The off state transistors maximize the path resistance and hence degrade the leakage current of the logic circuit. Additional inserted transistors increased the chip area and

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propagation delay of the logic circuit. In [9] authors developed SCCMOS technique to reduce the leakage current in standby mode by turning-off the transistor fully which connect the main circuit to power supply. The gate of the same threshold PMOS sleep transistor is at the potential which is higher than power supply V_{DD} voltage to stay the transistor in super cut-off condition. A strong charge pump circuit is required to sufficiently increase the gate voltage in an adequate time. The designing of capable charge pump circuit may cause extra power consumption, more area requirement and large propagation delay. J.C. Park and V.J. Mooney III in [10] combing the forced stack and MTCMOS technique. This provides the considerably control of leakage current and valuable for substantially delay declined in active mode. The drawbacks of this technique are large area penalty due to one transistor replaced by three transistors and additional managing circuitry required for sleep signals.

N. Hanchate and N. Ranganathan in [11] proposed a simple, single threshold and reliable technique. It uses two Leakage Control Transistors (LCTs) which are connected in such a way so that one of the LCTs is always near its cut-off for any combination of input signal. It reduces the leakage current in the path from V_{DD} to ground because one or more transistors are in cut-off mode and they act as large value resistance. In [12], the technique introduces two additional high threshold transistors in the logic circuit to introduce the concept of force stacking. In force stack arrangement the resistance of the leakage path increases and therefore reducing the leakage current. The difficulty of this technique is, the low signal is not exactly close to ground and the high signal is not exactly close to V_{DD}. The other difficulties are the propagation delay through the circuit increases due to reducing output voltage swing and implementation of two different threshold voltages on single chip. In [13] three sleep transistors are used for leakage reduction purpose as well as increasing the characteristics of the logic circuit. Two sleep transistors (a NMOS and a PMOS) are of the same threshold voltage as the logic circuit transistors have, while other third transistor (PMOS) has high threshold voltage. The high threshold voltage sleep transistor is connected between the pull-up and pull-down networks. The leakage current is controlled due to breaking of the path between pull-up and pull-down networks. The drawback of this leakage reduction technique is that it requires a controller to automatically control and generate sleep signals to put the circuit in standby mode and also to make active when it required.

III. Proposed ONOFIC Approach

On/Off logIC (ONOFIC) approach is a simple and single threshold voltage circuit level approach for reducing the leakage current and thus leakage power directly affected the total power dissipation of the logic circuit. ONOFIC approach is very efficiently reducing the both active as well as standby mode of leakage current. It used the extra insertion of a logic circuit between the pull-up and pull-down network for minimizing the leakage current. This extra inserted logic circuit is called On/Off logIC (ONOFIC) block. The ONOFIC block contains one NMOS and one PMOS transistor. The transistors in ONOFIC block are connected as shown in Fig. 2. The logic block is called ONOFIC because for any output logic level this logic block must be in on or in off condition. The precisely turning-on/off of ONOFIC block is directly affected the power dissipation and propagation delay of the logic circuit. The ONOFIC circuit using the concept of force stacking to provides the maximum resistance to the ONOFIC block when it is in off state and minimum resistance when it is in on state for controlling the leakage current. In ONOFIC block the PMOS transistor control the operation of the NMOS transistor. The ONOFIC NMOS/PMOS transistors must be in cut-off or in linear mode depending on the output logic.

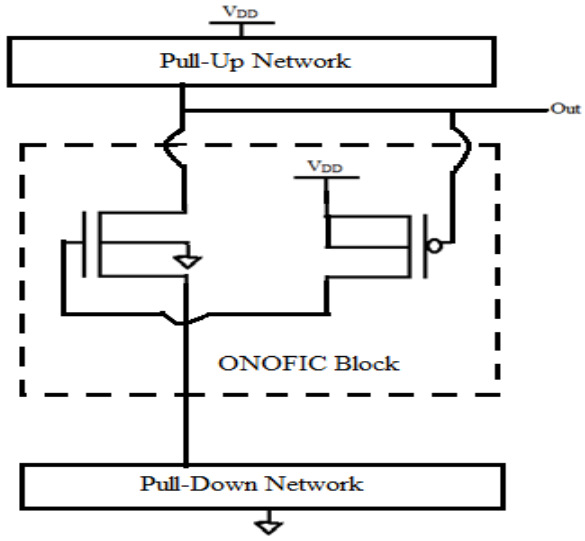

Fig. 2 ONOFIC Schematic

An extended ONOFIC approach called alternate ONOFIC is used to further reducing the leakage current of the logic circuits. It uses two ONOFIC blocks one at the side of pull-up network and another at the side of pull-down network. These two ONOFIC blocks are dual in nature and giving the logic low or logic high leakage reduction in alternate cycle of the input signal combinations. For any output stable level only one of the ONOFIC block is turn-on and other one should be in turn-off state. Alternate ONOFIC schematic is shown in Fig. 3. If input signal combinations are like that so the output is at logic low then the ONOFIC block below of output should be in conducting mode and both of its transistors are turn-on to create a conducting path from output to ground and stay the output at logic low stable condition. In the same way if input signals are like that so the output is at logic high then ONOFIC block above of the output should be in conducting mode and both of its transistors are turn-on to create a conducting path from power supply to output to stay the output at logic high level.

The transistors attach between the pull-up or pull-down network to output in ONOFIC logic circuits are called path transistors while the other transistors attach with output and control the input signal of path transistors are called forced

transistors. The operation of path transistors in ONOFIC block are controlled by the ONOFIC forced transistors. If the input of the path transistors is precisely managed by the forced transistors then ONOFIC block reduce the leakage current at manageable propagation delay of the logic circuits.

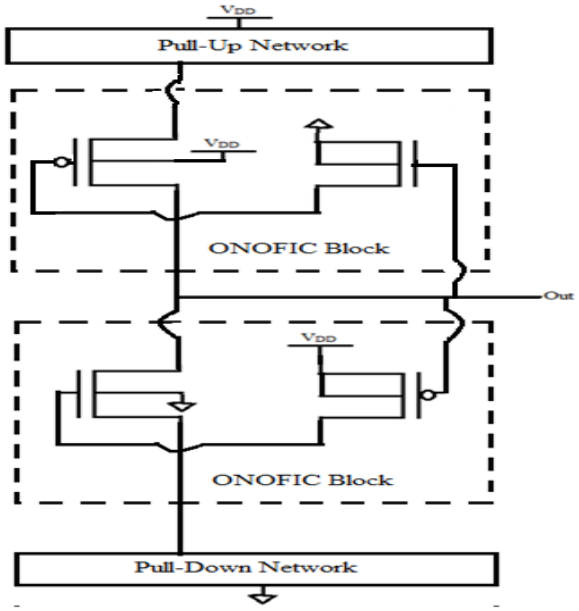

Fig. 3 Alternate ONOFIC Schematic

Table I explains the operation of ONOFIC CMOS NAND2 gate for reducing the leakage current. PMOS1 and PMOS2 are connected parallel in pull-up network while NMOS1 and NMOS2 are connected series in pull-down network. The focus point of this technique is its ideal on/off property. From Table I, the ONOFIC block is completely on or off for any combination of input signal. The control of ONOFIC block is depending on output signal of the logic circuit. If ONOFIC block is in on condition that shows both ONOFIC transistors are in linear region while in off state both transistors are in cut-off mode. When ONOFIC block is turned on then this block provides a nice conducting path and hence minimized the probability of leakage current while in its turn-off condition logic block has very high resistance and precisely control the leakage current. The idea for using the single threshold voltage is develop an easy and powerful leakage reduction technique without using the extra sleep or bias controller.

TABLE I
OPERATING STATUS OF THE TRANSISTORS IN THE ONOFIC CMOS NAND2 GATE

Inputs	PMOS1	PMOS2	ONOFIC PMOS	ONOFIC NMOS	NMOS 1	NMOS 2
(0,0)	On	On	Off	Off	Off	Off
(0,1)	On	Off	Off	Off	Off	On
(1,0)	Off	On	Off	Off	On	Off
(1,1)	Off	Off	On	On	On	On

IV. RESULTS AND DISCUSSION

In previous years many leakage reduction technique are used to manage the leakage current in deep submicron regime. Through literature survey we found a technique which also used the single threshold voltage throughout the circuit is LECTOR (LEakage Control transisTOR). So in this section we compare the results of ONOFIC approach to LECTOR technique to find the importance of ONOFIC approach.

A. DC Characteristic

The DC characteristic of conventional, LECTOR, ONOFIC and alternate ONOFIC CMOS inverter are shown in Fig. 4. We observed from Fig. 4 that the slope of the DC characteristic of ONOFIC and conventional CMOS inverter are nearly similar to each other and having the large slope while LECTOR CMOS inverter has low slope. The dc characteristic of alternate ONOFIC CMOS inverter is similar to conventional inverter. The output voltage swing and noise immunity in both conventional and alternate ONOFIC approach are the same as similarity in the dc characteristic. For any input combinations the slope of the CMOS inverter gate is given as (1).

$$Slope = {\partial \mathrm{Vout}}/{\partial \mathrm{Vin}} = {\partial(\mathrm{IoutRout})}/{\partial \mathrm{Vin}} \quad (1)$$

where

$$Iout = \frac{\mathrm{K}}{2}(\mathrm{VT})^2 \mathrm{e}^{(\mathrm{Vin}-\mathrm{Vth})/\mathrm{VT}}\left(1-\mathrm{e}^{-\frac{\mathrm{Vout}}{\mathrm{VT}}}\right) \quad (2)$$

Here k depends on process parameters of the device, VT is temperature dependence voltage. Vth is threshold voltage of the device and depends on the flat voltage, charge storing capacitance, doping densities of the material. Equations (1) and (2) show that the large slope is due to large Iout current which may cause large static power dissipation and therefore LECTOR technique has low static power dissipation as compare to conventional and ONOFIC approach. This plot simply indicates the lower leakage in alternate ONOFIC approach. The propagation delay is given as (3).

$$tp = {(Zout\Delta Vout)}/{\Delta Iout} \quad (3)$$

Zout shows the sum of resistive and capacitive loads of the CMOS circuit. From (3) ONOFIC and conventional circuits having the large Iout and thus propagation delays are the less as compare to LECTOR technique. Lower propagation delay gives the quicker response at the output while applying the input combinations.

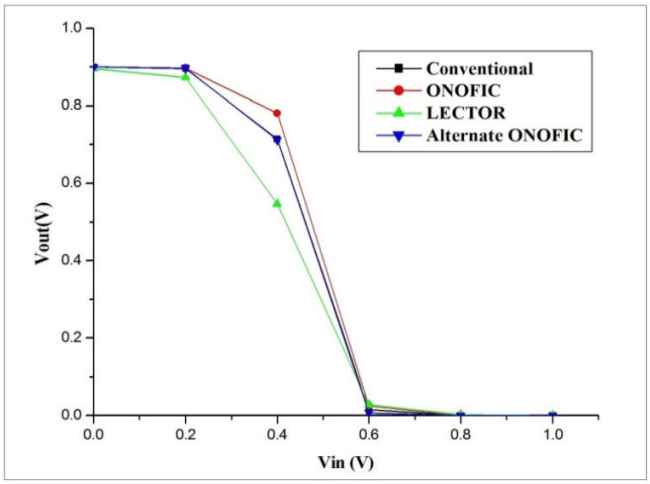

Fig. 4 DC Characteristic of CMOS inverter

Alternate ONOFIC approach has the propagation delay in between of the ONOFIC and LECTOR technique because its dc characteristic lying in middle of these two techniques. It has all characteristics similar to conventional CMOS circuit like noise immunity, output swing, fan-in, fan-out, current driving capability etc. at low power dissipation. Our proposed work gives the good compromise between leakage power and propagation delay for designing low power and high speed logic circuits.

B. Power Dissipation, Propagation Delay and Power Delay Product of Logic Circuits

In this section we compare our proposed ONOFIC approach with the conventional circuits and LECTOR technique. We analyzed the logic CMOS library cells like conventional, LECTOR and ONOFIC CMOS inverter, CMOS buffer, CMOS NAND2, CMOS NOR2, CMOS D-latch and CMOS 1-bit full adder circuits at 32nm technology. We calculate the power dissipation, propagation delay and Power Delay Product (PDP) for these logic circuits. We estimated the % saving of power dissipation, % increase in propagation delay and % change in the power delay product of the logic circuits with reference to conventional logic circuit. For our analysis purpose we used HSPICE tool and 32nm Berkeley Predictive Technology Model (BPTM) file. Table II shows the results for power dissipation, propagation delay and PDP of different CMOS circuits at 32nm technology node.

TABLE II
POWER DISSIPATION, PROPAGATION DELAY, POWER DELAY PRODUCT (PDP) OF CMOS LOGIC CIRCUITS AT 32NM TECHNOLOGY

Logic Circuit	Power Dissipation (nW)	% Saving of Power Dissipation	Propagation Delay (psec)	Propagation Delay Penalty	PDP (aJ)	% Change in PDP
Conventional Inverter	13.217	-------	183.31	-------	2.422	-------
LECTOR Inverter	4.382	66.85	581.19	3.17X	2.547	+5
ONOFIC Inverter	6.307	52.28	297.03	1.62X	1.873	-23
Alternate ONOFIC Inverter	5.461	58.68	494.78	2.70X	2.372	-2
Conventional Buffer	41.995	-------	308.88	-------	12.971	-------
LECTOR Buffer	19.933	52.53	656.89	2.13X	13.094	+0.9
ONOFIC Buffer	30.074	28.39	403.38	1.31X	12.131	-6
Alternate ONOFIC Buffer	21.030	49.92	582.31	1.89X	12.246	-6
Conventional NAND2	24.295	-------	215.34	-------	5.232	-------
LECTOR NAND2	9.933	59.12	595.66	2.77X	5.917	+13
ONOFIC NAND2	13.351	45.05	350.06	1.63X	4.674	-11
Alternate ONOFIC NAND2	11.865	51.16	468.83	2.18X	5.563	+6
Conventional NOR2	27.528	-------	261.44	-------	7.197	-------
LECTOR NOR2	10.362	62.36	741.52	2.84X	7.684	+7
ONOFIC NOR2	13.763	50.00	377.60	1.44X	5.197	-28
Alternate ONOFIC NOR2	11.359	58.74	537.38	2.06X	6.105	-15
Conventional D-latch	27.421	-------	259.73	-------	7.122	-------
LECTOR D-latch	17.632	35.70	466.98	1.80X	8.234	+16
ONOFIC D-latch	21.028	23.31	291.18	1.12X	6.123	-14
Alternate ONOFIC D-latch	18.164	33.76	349.41	1.35X	6.347	-11
Conventional 1-bit full adder	218.231	-------	864.40	-------	188.639	-------
LECTOR 1-bit full adder	149.463	31.51	1335.45	1.54X	199.600	+6
ONOFIC 1-bit full adder	174.181	20.19	1055.41	1.22X	183.832	-3
Alternate ONOFIC 1-bit full adder	160.547	26.43	1195.27	1.38X	191.897	+2

Table II represents that LECTOR technique is slightly good leakage reduction technique and can reduce more leakage current as compare to ONOFIC approach. The LCTs are attached in such a way to provide the high/low impedance path from voltage supply to ground as depends on input signals to reduce the leakage current. NAND type logic circuit implementation can improve the leakage power and propagation delay as compare to NOR type logic implementation. This is because of series connected transistors in pull-down network increased the critical current path from output to ground while having the full performance of the logic circuit [14]. ONOFIC approach reduces the less leakage power as compare to LECTOR because of no path breaker in pull-up circuitry.

It is needed to add some extra transistors in the logic circuit for minimizing and monitoring the leakage current. The extra inserted transistors may increase the chip area and propagation delay of the circuit. As LECTOR is a relatively good leakage reduction technique for designing the low power circuits but this technique is not capable to reduce the propagation delay and to get full output swing of the logic circuits. The logic synthesis of LECTOR is such that LCTs depends on their operation before giving the output response. ONOFIC leakage reduction technique is nicely reduced the leakage power and propagation delay as well. Table II shows that there are lot of differences in propagation delay between ONOFIC and LECTOR technique.

The large power delay product deals with the large figure of merit of the logic circuits. In deep submicron region, the power dissipation and propagation delay both are increased. The incremental of propagation delay is due to inversely dependency on the trans-conductance of the relative transistor. The incremental of power dissipation is due to proportional dependency on the leakage current in deep submicron regime. The least value of PDP is obligatory for better performance of logic circuits [15].

From Table II we show that our proposed technique has lower PDP than conventional and LECTOR technique. The + and – signs represents the power delay product is increasing or decreasing with respect to conventional circuits. ONOFIC technique has the negative power delay product which simply indicates that the ONOFIC logic circuits have the lower PDP than the conventional logic circuits. The ONOFIC approach has the good figure of merit and may be used as a dominant leakage reduction technique for deep submicron CMOS circuits.

C. ONOFIC Transistors Leakage Current

The behavior of ONOFIC block transistors paid an important role to control the leakage current. Fig. 5 investigated the effect of input voltage variation on the ONOFIC transistor's leakage current in CMOS inverter at 32nm technology node.

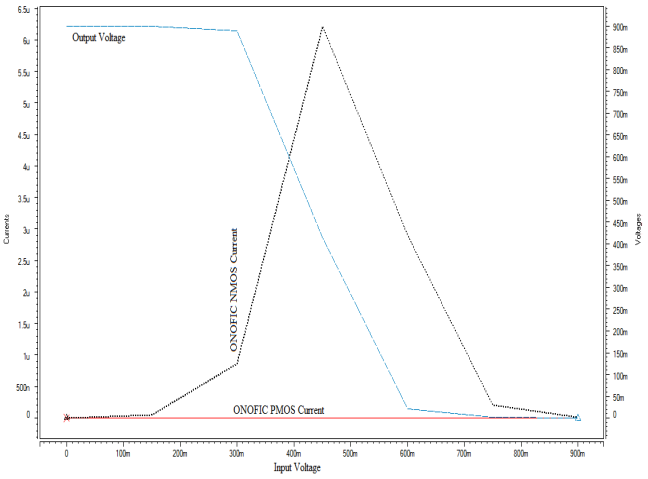

Fig. 5 ONOFIC transistors current

PMOS ONOFIC transistor behaves as a high-quality switch because having low leakage current for turning on or turning off the NMOS ONOFIC transistor. It has negligible change in current during output signal transition. NMOS ONOFIC transistor has more than 6μA current during the output signal transition. For making an ideal NMOS ONOFIC transistor the change in current must be minimized. The proper biasing of the NMOS ONOFIC transistor can do this task carefully.

D. Effect of ONOFIC Power Supply

Fig. 6 explains the effect of supply voltage of the ONOFIC block on the output of the NAND3 gate at technology 32nm. Let us give the different voltage supply V_{DD1} for the ONOFIC block rather than main circuit power supply V_{DD}. When V_{DD1} is '0' the output voltage is not on logic low while input signal is at logic high. This choice of power supply degrades the presentation of the logic circuit but quite saving in power dissipation. As slowly moves to high power supply of ONOFIC block, it improves the output signal presentation. The switching threshold voltage of the logic circuit is come in ideal condition i.e. half of the power supply V_{DD} when the power supply of main circuit and power supply of ONOFIC block is equal.

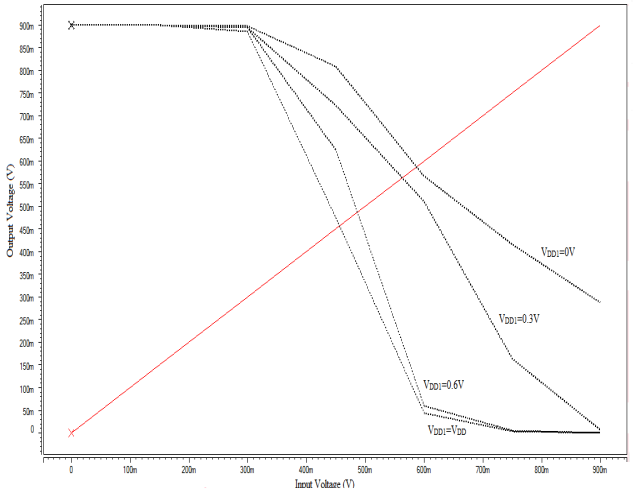

Fig. 6 Effect of Supply Voltage variation of ONOFIC block

E. Temperature Effect on Output Voltage and Leakage Current of ONOFIC Block

In Fig. 7, the effect of temperature variation is shown on the output voltage and on the ONOFIC transistors leakage currents. As temperature increases the output voltage and ONOFIC NMOS transistor current both are reduce. The variation in output voltage and ONOFIC PMOS transistor due to temperature variation is negligible. The graph shows the negligible effect of temperature when output state of the logic circuit is at stable level and quietly affected the logic circuit when output state comes in transition region.

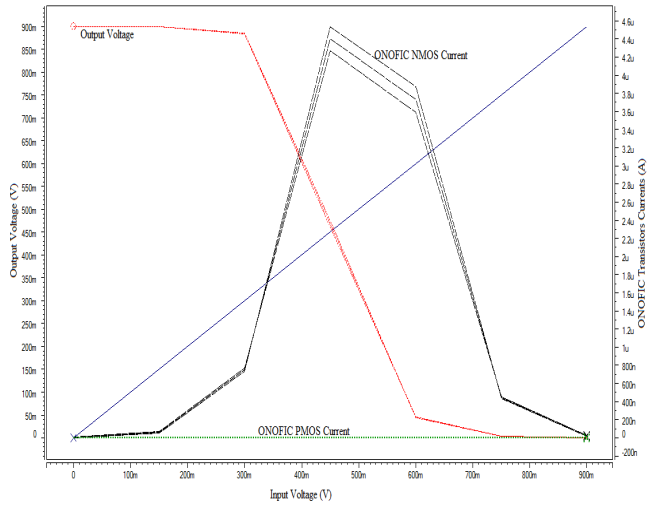

Fig. 7 Temperature effect on the Output Voltage and on ONOFIC transistors Current

F. Sizing of ONOFIC Transistors

The sizing of the ONOFIC transistors is the important concern of this technique. Efficient and proper sizing of the ONOFIC transistors gives the better results. The transistors in ONOFIC block are sized to study the effect on power dissipation and propagation delay. Multiply number with technique, indicates that the widths of corresponding ONOFIC block transistors are the times of pull-up/down NMOS and PMOS transistors in the logic circuit respectively.

It can be observed from Fig. 8 that as the widths of ONOFIC transistors are increased the power dissipation also increased as the leakage current is proportionally depends on the feature size of the transistors therefore reduction in % saving in power dissipation of the logic circuit. The benefits of increased sizing of the transistors are the reduction in the propagation delay and hence enhance the speed of the logic function.

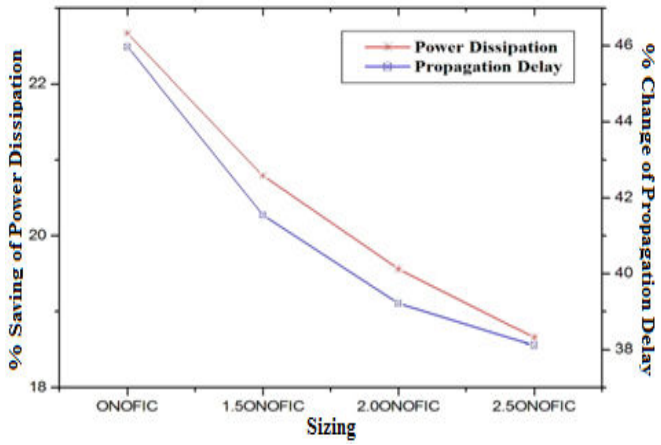

Fig. 8 Sizing effect of ONOFIC transistors in NAND3 gate at 32nm technology

V. Conclusion

ONOFIC approach reduces the leakage power and enhances the performance of the logic circuits. This approach is the simple and single threshold voltage technique and eliminates the restrictions of complexity, monitoring system and poor speed of the logic circuits as compare to other leakage reduction techniques. In this article we compare ONOFIC approach to LECTOR technique as LECTOR is also used the single threshold voltage extra inserted transistors. Therefore by taking CMOS library logic cells we concluded that our approach gives the better result in terms of low power and high speed integrated circuits implementation as compare to LECTOR technique. The improved PDP is the important feature of this approach and open the path for future deep submicron logic implementations.

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