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A Resistorless High Input Impedance First Order All-Pass Filter Using CCCIIs

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***Abstract*—**A new first order all-pass filter topology realized using current controlled current conveyors (CCCIIs) is introduced in this paper. Offered benefits are the high-impedance of the input node, the absence of external resistors because of the usage of CCCIIs with positive and negative intrinsic resistances, the presence of only grounded capacitors, and the capability of electronic adjustment of the phase shift through a single bias current. The correct operation of the introduced topology is conformed through simulation results, while its behavior is evaluated through comparison results.

***Keywords*—**Active filters, All-pass filters, Analog signal processing, Current conveyors.

I. Introduction

THE second-generation current conveyors (CCIIs) are widely used as active elements for performing analogue signal processing, due to the offered capability for operation at higher frequencies than those achieved by the conventional op-amp configurations. In addition, CCIIs offer design flexibility that is originated from their terminals properties [1]-[6].

Attractive CCIIs configurations have been already proposed in [3] and [6]. More specifically, a CCII with positive intrinsic resistance has been introduced in [3], while a CCII configuration with negative intrinsic resistance has been presented in [6]. The main benefit of the aforementioned CCIIs is that their parasitic resistance associated with the low impedance input node (node X) can be electronically controlled by the bias current. As a result, these structures are known in the literature as current-controlled current conveyors, denoted as CCCII+ [3] and CCCII^{+} [6], respectively.

First order all-pass filters are very useful building blocks for providing a phase shift between the input and output signals. Thus, a significant research effort has been done in order to derive all-pass filter structures by employing CCIIs. A number of first order all-pass filter topologies have been introduced in [7]-[12]. All the above topologies have the drawback of the absence of a high impedance input node, leading to the requirement for employing additional circuitry in the case that this type of filters would be embedded in a high order system.

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In [13], a high-input impedance first order all-pass filter topology has been introduced, where a grounded capacitor and a floating external resistor are required in the case that the two employed CCIIs become current controlled. Thus, electronic tuning is not offered by this topology. In [14], a high-input impedance first order all-pass filter topologies have been also introduced. These topologies cannot be made resistorless using CCCIIs due to presence of a resistor connected at their output. In [15], a high input impedance all-pass filter topology is presented constructed from a CCCII and an operational amplifier. Thus, it is obvious that this topology has a limited maximum frequency of operation imposed by the compensation scheme of the operational amplifier. In addition, a floating capacitor is used making this topology not suitable in the integration point of view due the limitation imposed by the parasitic capacitors at high frequency applications. In [16], one of the introduced topologies has the benefit of high input impedance. This could be achieved by employing a CCCII-, an external floating resistor, and a floating capacitor. From the realization point of view, CCCII+ is more preferable than the CCCII- and, also, floating capacitors impose restrictions in high-frequency applications.

In this paper, a novel first order all-pass filter using three CCCIIs is proposed. The proposed circuit offers simultaneously the following advantages: high input impedance, employment of only grounded capacitors, resistorless realization, and phase shift tuning by varying a single bias current. The paper is organized as follows: in Section II the novel all-pass filter configuration is introduced, while its behavior is evaluated in Section III through simulation results. In order to be evident the benefits offered by the new topology a comparison with the already published structures is also performed.

II. Proposed All-Pass Filter Configuration

The proposed all-pass filter configuration is given in conceptual form in Fig. 1.

Assuming that $R_1=R_2\equiv R$ and by performing a routine algebraic analysis it is derived the following transfer function

$$H(s)=\frac{RCs-1}{RCs+1} \tag{1}$$

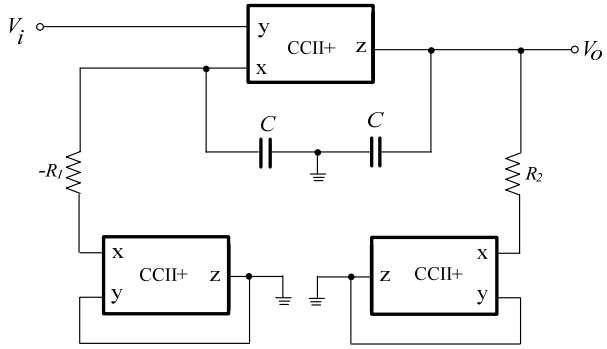

Fig. 1 Conceptual representation of the proposed all-pass filter topology

Attractive features offered by the proposed filter are the following:

a) The high-impedance of the input nodes facilitates cascading for deriving high order filter topologies, due to the fact that there is not loading effect between the input of the configuration in Fig. 1 and the output of a preceding stage.
b) The requirement of only grounded capacitors gives potential for implementing the proposed filter topology in integrated circuit form without any restriction imposed by the parasitic capacitances at high-frequencies.
c) The proposed configuration can become resistorless in the case that the CCCIIs introduced in [3] and [6] would be employed. In addition, its frequency behavior can be electronically adjusted through a single bias current implemented as in [17].

In order to demonstrate the claims given in c) the topology in Fig. 1 is redrawn as it is depicted in Fig. 2, where CCCIIs are now employed. By performing a simple inspection of the topologies given in Figs. 1 and 2 and taking into account that the parasitic resistance associated with node X of a CCCII is given by the expression $R_X=V_T/2I_o$, where V_T is the well-known thermal voltage and I_o is the bias current, it is concluded that the negative resistance R_1 is implemented by the CCCCII+ and the positive resistance R_2 is implemented by the rightmost CCCII+. With regards to the parasitic resistance at node X of the leftmost CCCII+, it can be realized much smaller than that of the CCCII+ by choosing a relative large value of the corresponding bias current I_{o1}.

Also, note that as the resistances associated with X terminals of the CCCII+ and the rightmost CCCII+ are equal and, as a result, they can be controlled by a single bias scheme as that proposed in [17]. As a result, single element phase shift is offered by the proposed topology.

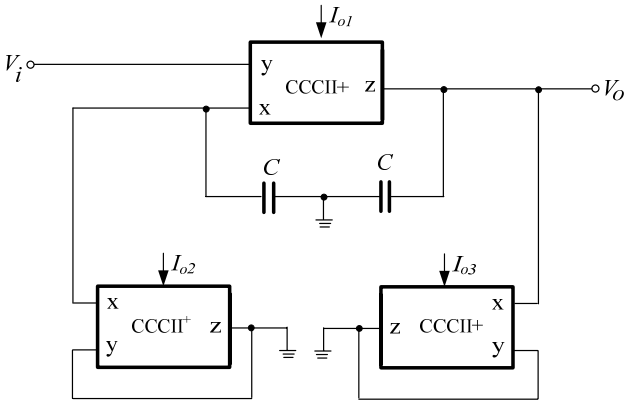

Fig. 2 Proposed all-pass filter realized by employing CCCII+ and CCCII+

III. Simulation and Comparison Results

The correct operation of the topology in Fig. 2 has been verified through SPICE simulation results. For this purposed, the topologies introduced in [3] and [6] with symmetrical power supply voltages ±2.5V have been employed in the simulations.

The bias currents I_{o2} and I_{o3} have the same value 13μA, while the value of the current I_{o1} has been chosen equal to 650μA in order to minimize the effect of the corresponding parasitic resistance. The value of the capacitor was equal to 1.5nF. The simulated gain and frequency responses, obtained by considering BJT model parameters provided by AT&T, are simultaneously plotted in Fig. 3. The observed deviations in the gain response at low frequencies are caused by the parasitic elements introduced by the employed transistor models.

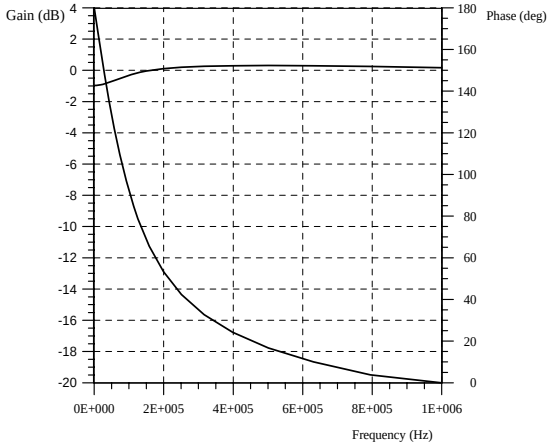

Fig. 3 Simulated gain and phase responses of the filter in Fig. 2

TABLE I
COMPARISON RESULTS FOR THE PROPOSED ALLPASS FILTER

Filter	Without resistors	External resistors	Grounded capacitors	Capacitors	CCCIIs
[16]	NO	1 floating	NO	1	1 CCCII-
[13]	NO	1 floating	YES	1	2 CCCII+
[14]	NO	1 grounded	YES	2	2 CCCII+
[14]	NO	1 grounded	YES	2	1CCCII- 1 CCII+
Fig. 2	YES	0	YES	3	1 CCCII$^+$ 2 CCCII+

In order to facilitate our discussion the comparison results concerning some important performance characteristics of the proposed topology and those already published are summarized in Table I. The main conclusions obtained from this table are the following:

a) With regards to the topology introduced in [16] the main offered benefits are the capabilities for resistorless implementation, for electronic adjustment of the phase shift through a single bias current. A floating capacitor is used in the [16], while only grounded capacitors are employed in the propose filter topology. In addition, the transistor-level implementation of floating resistor that is required in the topology under comparison is not an easy procedure in practice. Also, note the requirement for a CCCII- instead of a CCCII+; it is known that plus type CCIIs are more preferable than the minus type CCIIs. On the other hand, the number of the required CCCIIs and capacitors is increased in the proposed topology.

b) With regards to the topology introduced in [13] the offered benefits are the resistorless implementation and the capability of electronic phase shit by adjusting a single bias current. A floating external resistor is required in [13] and this does not facilitate the implementation of this resistor in active circuit form. Note also that, in order to achieve implementation using only CCCIIs, the bias current one of the CCCIIs employed in [13] must be larger than that of the other CCCII as in the case of the proposed topology. On the other hand, the number of the required CCCIIs is increased in the proposed configuration and, also, two grounded capacitors are employed instead of one grounded capacitor used in [13].

c) With regards to the topologies in [14] the offered benefits are the resistorless implementation and the possibility of electronic phase shit by adjusting a single bias current. Also, plus and minus type of CCCIIs are employed in the second topology of [14] and this is not an advantage in the actual implementations. Note also that, in order to achieve implementation using only CCCIIs, the bias current one of the CCCIIs employed in [14] must be greater than that of the other CCCII as in the case of the proposed topology. The price paid is that the number of the required CCCIIs is increased in the proposed configuration.

IV. CONCLUSION

A novel all-pass filter configuration has been proposed which has the advantages of high input impedance, resistorless realization, employment of grounded capacitors, and electronic phase shift tunability through a single bias current. On the other hand, the price paid is that the number of the employed CCCIIs is increased in comparison with the corresponding already published structures. The proposed all-pass filter configuration could be used for achieving high-performance analogue signal processing. Conclusion section is not required. Although a conclusion may review the main points of the paper, do not replicate the abstract as the conclusion. A conclusion might elaborate on the importance of the work or suggest applications and extensions.

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