World Academy of Science, Engineering and Technology
International Journal of Electrical and Computer Engineering
Vol:3, No:4, 2009

A New Performance Characterization of Transient Analysis Method

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***Abstract*—**This paper proposes a new performance characterization for the test strategy intended for second order filters denominated Transient Analysis Method (TRAM). We evaluate the ability of the addressed test strategy for detecting deviation faults under simultaneous statistical fluctuation of the non-faulty parameters. For this purpose, we use Monte Carlo simulations and a fault model that considers as faulty only one component of the filter under test while the others components adopt random values (within their tolerance band) obtained from their statistical distributions.

The new data reported here show (for the filters under study) the presence of hard-to-test components and relatively low fault coverage values for small deviation faults. These results suggest that the fault coverage value obtained using only nominal values for the non-faulty components (the traditional evaluation of TRAM) seem to be a poor predictor of the test performance.

***Keywords*—**testing, fault analysis, analog filter test, parametric faults detection.

I. Introduction

THE rapid development of integration technologies has allowed the implementation of very complex analog and mixed-signal integrated circuits. It has been found that the test of analog sections significantly affects the global manufacturing cost, even if these sections generally represent a small fraction of the total circuit area [1]. This fact motivates the implementation of new test strategies. In addition, the usually low observability of the internal nodes and the complex nature of the involved signals make the analog testing a very challenging task [2].

In order to reduce test costs, considerable research work addresses the structural testing of the subsystems commonly used in analog and mixed signal applications. Particularly, some researchers targeted continuous and discrete time filters and developed test strategies usually based on circuit reconfiguration and addition of extra circuitry [1].

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The Transient Analysis Method (TRAM) has been proposed for testing second order filters [3], [4].TRAM is a very appealing test method due to its high efficiency and relatively straightforward implementation. The core idea of this strategy is to excite the Circuit Under Test (CUT) with an input signal that causes an under-damped output transient, assuming that a fault in the CUT will change the peak time and/or the overshoot. TRAM has been suggested as a functional test methodology because the monitored parameters in test mode are related to two functional specifications of the CUT.

The ability of TRAM for detecting single deviation-faults in the filter components has also been evaluated, reaching 100% of fault coverage. This high fault coverage is computed assigning nominal values for non-faulty components, a simplification that allows implementing fault simulations in a very straightforward way. However, the metrics obtained following this approach do not take into account the natural variability of devices caused by many factors, such as manufacturing processes, aging and surrounding environment. This fact could lead to fault coverage values that overestimates or underestimates the efficiency of the test scheme.

In this work, we propose a new performance characterization of TRAM. Using a more realistic fault model and Monte Carlo simulations, we obtain metrics for qualifying this test strategy. The new data reported here reveal some limitations of this test strategy not observed in previous work, like poor ability for detecting small deviation faults and the presence of hard to test components.

II. Parametric Fault Models

Traditional fault models consider that a single catastrophic or deviation fault can occur in a given CUT component while the remaining ones adopt their nominal values. In this paper, parametric faults are defined as out-of tolerance deviations in the process, circuit o system parameters [5]. For detecting parametric faults, the statistical deviations in the values of the fault-free components should be considered in order to obtain a more accurate evaluation of the test technique under study.

Several researchers have devoted their efforts in formulating new fault models and simulation techniques for analog circuits. The authors of [6] propose two fault models: single-fault and group-fault. In the first case, it is considered that all circuit parameters can fluctuate within their tolerance

limits and only one adopts a value outside these limits. In the second case, a group of components is allowed to adopt a value outside their tolerances. A similar single fault model and an algorithm for reducing the computational cost of fault simulations are proposed in [7]. Other researchers [8] related this model with the specifications in order to remove some of them for reducing the test time.

The authors of [9] inject faults in the low-level parameters of the CUT. A faulty parameter presents two probability distributions at both sides of its fault-free probability distribution. The remaining parameters vary within their tolerances. For each circuit instance, the authors concurrently determine the fulfillment of the specifications and the test attributes. They declare a given circuit as faulty if the deviations in the low-level parameters produce at least one specification going outside its tolerable limits. This approach allows the use of metrics for evaluating the test quality, such as yield coverage or fault coverage.

In [5], a model assuming Gaussian distributions for fault-free parameters and a uniform distribution for the faulty parameter is proposed. The detectability of a given fault is evaluated by analyzing the statistical distributions of the test attributes obtained using the above mentioned fault model.

The authors in [10], [12] employ multiple-deviation fault-models to evaluate the efficiency of test strategies (different from functional test) for discriminating out-of-specification circuits. For this task, they assume that the low-level circuit parameters present a Gaussian distribution, and consider different test scenarios by means of increasing the variability of the parameters.

Other authors [13]-[14], define several metrics for evaluating the efficiency of test strategies under the hypothesis of parametric faults.

III. Overview of TRAM

Even if this paper does not discuss TRAM implementation, for the sake of clarity this section presents some basic concepts related to this aspect of TRAM. Further details can be found elsewhere [3], [4].

As previously stated, TRAM monitors the peak time (Tp) and the overshoot (OS) of the filter under-damped transient response. These attributes have been depicted in Fig. 1, which shows the nominal ramp response of a band-pass filter. In order to simplify the analysis, we assume that all the test measurements are noise-free.

The values of test attributes (Tp and OS) can be obtained by evaluating expressions (1) and (2). In these expressions, ω_p is the undamped natural frequency and ζ is the damping ratio. These values characterize a second order dynamic system [3].

$$Tp = \frac{\pi}{\omega_p \cdot \sqrt{1-\zeta^2}} \ , \tag{1}$$

$$OS = e^{-\pi \frac{\zeta}{\sqrt{1-\zeta^2}}} \ . \tag{2}$$

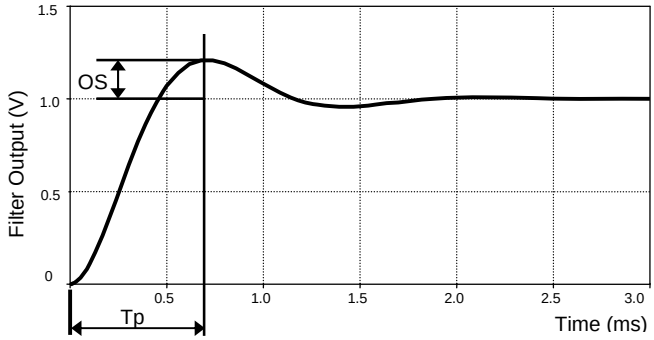

Fig. 1. Nominal ramp response of a band-pass filter

A simple analysis of the CUT topology allows establishing the relations between Tp and OS and the filter components (resistances and capacitors). In this way, it is possible to evaluate analytically the effects of the components variations in the test attributes and to perform fault simulation. Another possibility is directly measure the values of Tp and OS from SPICE simulations, but this alternative presents a higher computational cost than the direct evaluation of the expressions (1) and (2).

IV. Fault Simulation Procedure

A. Limits of test attributes for the fault-free circuit

The test attributes exhibit a band of possible values for the fault-free circuit due to the variations in the circuit parameters inherent to the manufacturing process. The limits of these bands are used for determining if a given fault can be detected by TRAM. For establishing these limits, it is necessary to characterize the statistical distributions of Tp and OS.

For this purpose, we model every circuit parameter (capacitors and resistances) as normally distributed random variable with a standard deviation characteristic of the manufacturing process. With these data, we implement a 1000-sample Monte Carlo simulation to obtain the Tp and OS values for each element of the sample. From the simulation results, we build the histograms of Tp and OS (shown in Fig. 2 for Filter 1, to be described in Section V). The size of the sample is subject to a trade-off between computational cost and precision of the results, and can be redefined according to the application needs.

Once the fault-free distributions are obtained, the Shapiro-Wilk test is used for determining the matching of the simulation results to Gaussian distributions. If the hypothesis of data normality cannot be rejected (at a certain confidence level) then we set the fault-free limits for Tp and OS as:

$$\mu_{Tp} - k \cdot \sigma_{Tp} \, ; \mu_{Tp} + k \cdot \sigma_{Tp} \tag{3}$$

$$\mu_{OS} - k \cdot \sigma_{OS} \, ; \mu_{OS} + k \cdot \sigma_{OS} \ . \tag{4}$$

The limits in (3) and (4) are denominated Statistical Tolerance Limits (STL). In these expressions, μ_{Tp} and μ_{OS} are the means of Tp and OS distributions respectively, whereas σ_{Tp} and σ_{OS} are their corresponding standard deviations. The k

value is chosen according to the percentage of the population values to be contained by the intervals, at a certain confidence level [15]. For instance, based on the 1000-sample Monte Carlo simulation, the 99.0% of the population will be within the band determined by (3) and (4) with k = 2.676, at a 95% confidence level.

If the hypothesis of data normality is rejected, it is possible to set limits independently of the distribution of the simulation results. However, for obtaining the same percentage of the population at the same confidence level, these limits usually require a sample size bigger than the required when the limits are established under normality assumption [15].

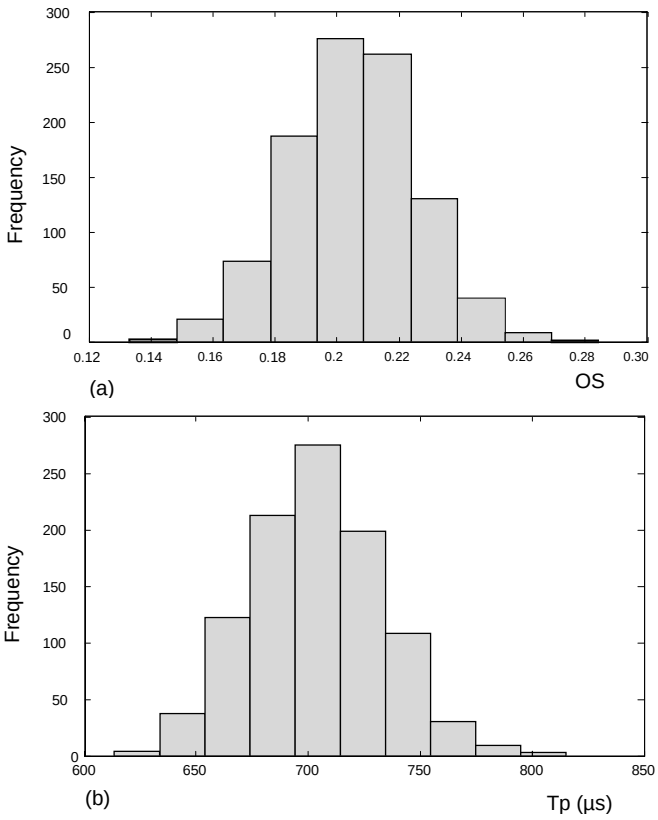

Fig. 2. Histograms of OS (a) and TP (b) fault-free values for Filter 1

It should be noted that the decision regarding the setting of limits is subject to statistical error. Once the limits for accepting (or rejecting) a circuit are established, two errors appear: one of them is to reject a circuit when is fault-free, the other is to accept a circuit when is faulty. From standard hypothesis testing, the first error is known as Type I error and the second one Type II error [16]. Moving the limits only produces a decrement of one of the errors at the expense of increasing the other, and is not possible to reduce both error probabilities simultaneously [6]. For illustrative purposes, Fig. 3 depicts hypothetical distributions for a fault-free circuit and a faulty one, with both errors indicated. The area of these error zones represents the corresponding probability error.

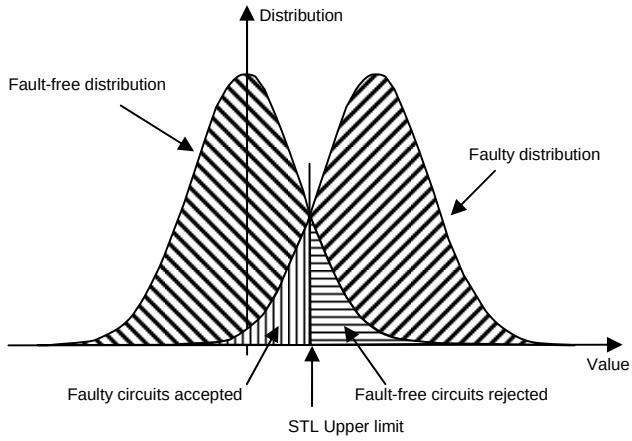

Fig. 3. An example of fault-free and faulty statistical distributions

B. Adopted fault model

For evaluating the ability of TRAM for detecting deviation faults in the passive components, we adopt the fault model proposed by Saab et al. [6]. This model considers that only one component can be faulty while the others adopt random values within their tolerance bands (obtained from their statistical distributions). The fault is introduced by assigning to the faulty component a deterministic value outside its tolerance band. Fig. 4 illustrates this concept for the C_1 component. In our experiments, we consider deviation faults (*df*) from ±10% up to ± 40% of the component nominal value, in steps of ±2.5%. Each deviation corresponds to a separate fault.

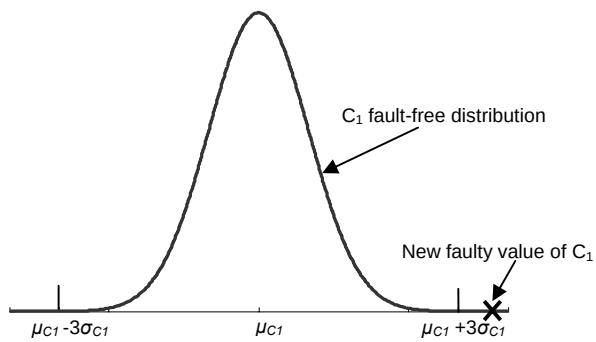

Fig. 4. Fault-free and faulty distribution of C1 component

C. Fault detection probability

For estimating the fault detection probability of a given deviation-fault, a 1000-individuals (filters) sample is generated. Each individual is characterized by n+r circuit parameters *ci*, such that

$$ci \in \{R_1, R_2, ..., R_n, C_1, C_2, ...C_r\}. \quad (5)$$

The individuals of the generated sample (instances of the CUT) are obtained by assigning a fixed value (a *df* fault) to the faulty circuit parameter, while the others adopt random values (with Gaussian distribution) within their tolerances. For this sample, we determine the number of individuals

presenting test attributes beyond the STLs, and declare them as detected. Then we use the following estimator:

$$FDP_{ci}(df_j) = \frac{NDF}{NIF} \ . \tag{6}$$

In (6) , $FDP_{ci}(df_j)$ denotes the probability of detecting the *jth* deviation fault (df_j) injected in the circuit parameter *ci* (that belongs to the set of n+r components), *NDF* is the total of the detected faults and *NIF* is the total of the injected faults (equivalent to the dimension of the generated sample). In this way, it is possible to obtain a set of plots depicting the ability of the test scheme for detecting deviation faults in the circuit components.

In order to obtain a test metric for globally characterizing TRAM, we adopt the one suggested by Khouas and Derieux [7]. The fault coverage is defined as the average of the fault detection probabilities obtained for each level of deviation. In (7), $FC(df_j)$ is the fault coverage for the df_j deviation fault, and $n+r$ is the number of components considered in the fault injection, and the summation is made for all the *ci* components.

$$FC(df_j) = \frac{\sum_{ci} FPD_{ci}(df_j)}{n+r} \ . \tag{7}$$

It should be noted that this metric allows a global evaluation of TRAM, but it is not useful for exposing the hard-to-test components.

V. Simulation Results

A. Filters under study

In order to estimate the performance of TRAM for detecting the targeted faults, we select two filters as cases of study. The first one is a second-order band-pass filter [17], and it is referred as Filter1 (Fig. 5). The second one is a low-pass filter [18] and it is referred as Filter 2 (Fig. 6).

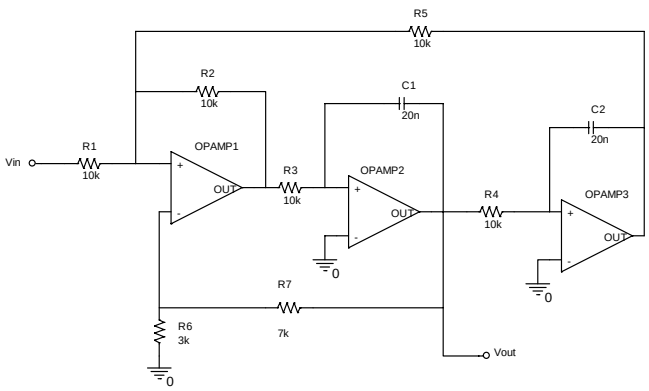

Fig. 5. First filter under test (Filter 1)

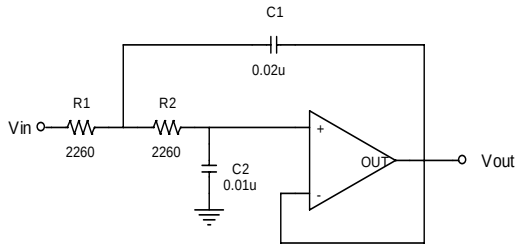

Fig. 6. Second filter under test (Filter 2)

In order to employ the expressions (1) and (2) for evaluating Tp and Os, we use (8) and (10) for relating ζ_1 and ω_{p1} with the circuit parameters of Filter 1, and (9) and (11) for relating ζ_2 and ω_{p2} with the circuit parameters of Filter 2.

$$\zeta_1 = \frac{R_6 \cdot (R_5 R_1 + R_2 R_5 + R_2 R_1)}{2 \cdot C_1 R_3 R_5 R_1 \cdot (R_6 + R_7)} \cdot \frac{1}{\sqrt{\frac{R_2}{C_2 R_4 C_1 R_3 R_5}}} \ , \tag{8}$$

$$\zeta_2 = \sqrt{\frac{C_2}{4 C_1 R_2 R_1}} \cdot (R_1 + R_2) \ , \tag{9}$$

$$\omega_{p1} = \sqrt{\frac{R_2}{C_2 R_4 C_1 R_3 R_5}} \ , \tag{10}$$

$$\omega_{p2} = \sqrt{R_1 R_2 C_1 C_2} \ . \tag{11}$$

With the aim of evaluating the ability of these expressions for predicting the values of the test attributes, we compare SPICE simulation results with the obtained using (1) and (2) and observe a very good matching between them. This motivates the use of these expressions for our evaluation procedure. In this way, the computational cost related to fault simulations is considerably reduced.

For establishing the limits of the test attributes for the fault-free circuit, we consider that the circuit parameters (for both filters) present Gaussian distributions. For the sake of simplicity, we use for the components a standard deviation of 3.333% of its nominal values, and perform a 1000-sample Monte Carlo analysis. In this way, it is possible to obtain from the generated data the statistical distribution of the test attributes.

The normality test applied to these distributions shows that it is not possible to reject the hypothesis of data normality with a confidence of 95%. Consequently, we assume for both filters that Tp and OS present Gaussian distributions and establish the STL depicted in Table I, taken under the consideration that the 99% of the observations obtained in the fault-free circuit simulation are within the band determined by the above-mentioned limits, with a confidence of 95%. The election of these limits diminishes the probability of rejecting a fault-free filter (Type I error).

TABLE I
STATISTICAL TOLERANCE LIMITS FOR TP AND OS

Statistical Tolerance Limits	*Filter 1*		*Filter 2*	
	Tp (s)	OS	Tp (s)	OS
Upper limit	7.8476E-04	0.2596	1.554E-4	0.058
Lower limit	6.2376E-04	0.1514	1.289E-4	0.028

B. Discussion of simulation results

1) Filter 1

For clarity purposes, we first present figures depicting $FDP_{ci}(df_j)$ for each component in the circuit. The results can be observed in Figs. 7 to 15. In these figures, the fault detection probability of every component (FDP_{ci}) is plotted versus the deviation fault injected (df_j) in the component. Three test alternatives are taken into account: Tp-only monitoring, OS-only monitoring and Tp-OS monitoring.

From Figs. 7 to 13 (resistors), it is possible to observe that both measurements (Tp and OS) are complementary because the deviation-faults are easily detected by monitoring OS in some cases but others require the Tp monitoring. A similar behavior is observed for the circuit capacitors (Figs. 14 and 15). This allows concluding that both measurements are required for obtaining high values of FDP_{ci}. The FDP_{ci} obtained considering the simultaneous monitoring of the two test attributes are also depicted in the above-mentioned figures.

It should be noted that a common behavior is observed from our simulation results: positive deviations in the value of the components are harder to detect than the corresponding negative ones. Additionally, our results show the relatively low efficiency for detecting small deviation-faults (20%). Reasonable FDP_{ci} are obtained for deviations faults higher than 35%, with the exception of R_1 (Fig. 7) and R_2 (Fig. 8) that should be considered as hard-to-test components using the test technique under study.

The fault coverage (Table II) shows low values for small deviation-faults (±20%), near to 55%. This confirms our previous observation about this kind of faults. By other hand, deviation faults of -30% and +40% produce acceptable fault coverage. For comparing our results with previously reported ones, it is necessary to obtain the global fault coverage. For this purpose, we consider only deviation faults of ±20% and ±40%, following the above mentioned procedure. In this way, fault coverage of 70.28% is obtained. This value is considerably lower that the obtained by other authors using a different fault model [4].

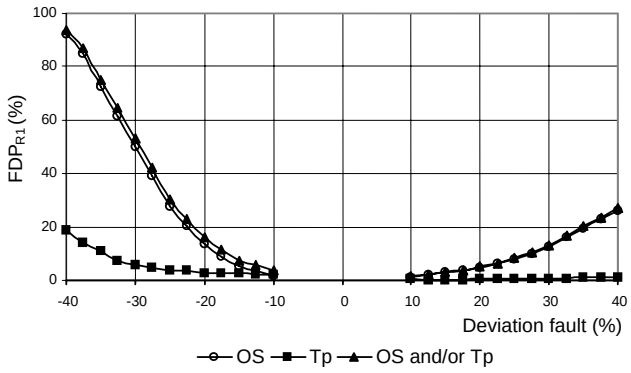

Fig. 7. R1 fault detection probability (Filter 1)

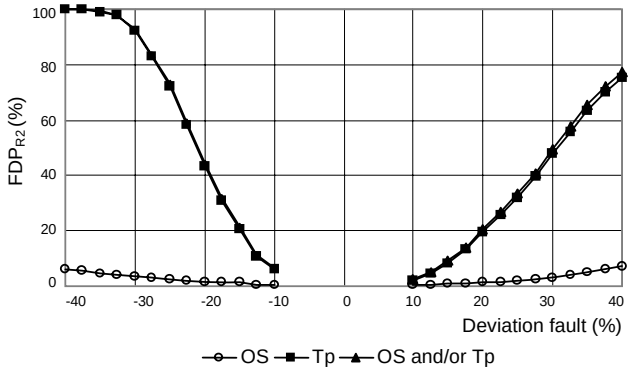

Fig. 8. R2 fault detection probability (Filter 1)

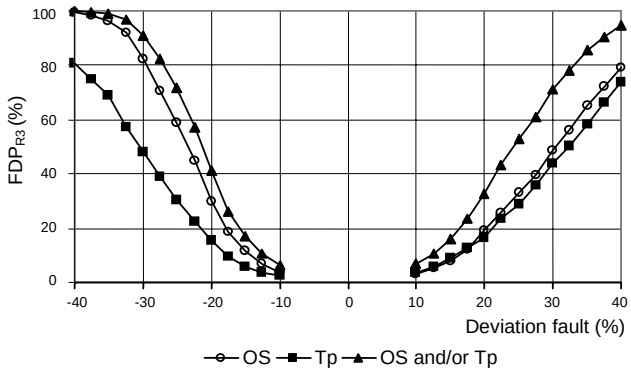

Fig. 9. R3 fault detection probability (Filter 1)

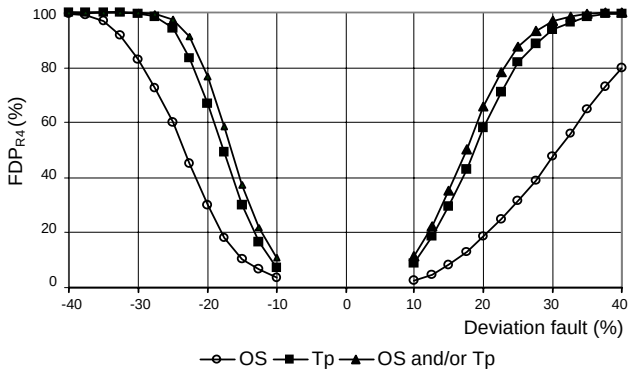

Fig. 10. R4 fault detection probability (Filter 1)

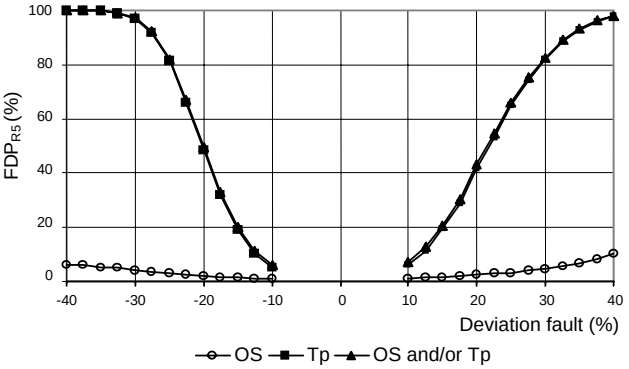

Fig. 11. R5 fault detection probability (Filter 1)

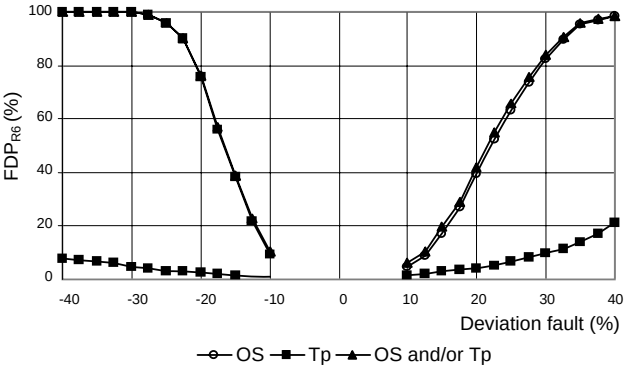

Fig. 12. R6 fault detection probability (Filter 1)

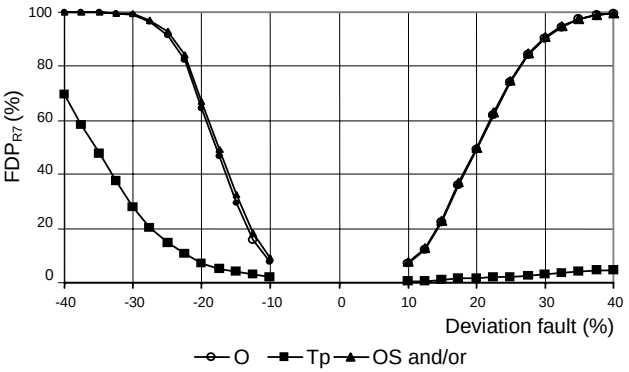

Fig. 13. R_7 fault detection probability (Filter 1)

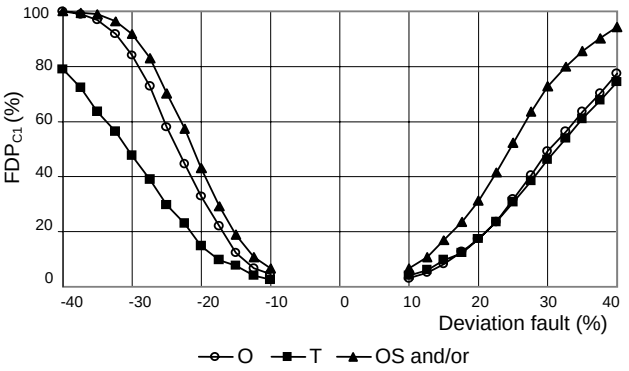

Fig. 14. C1 fault detection probability (Filter 1)

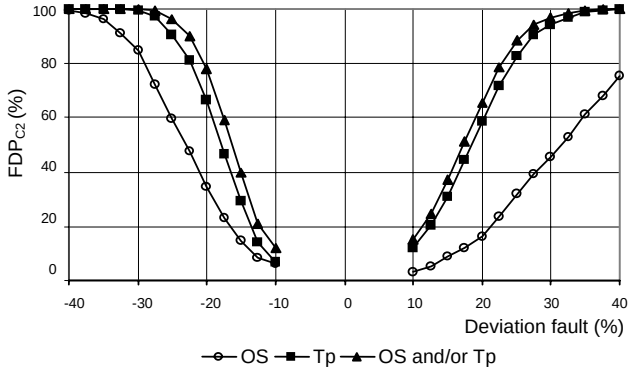

Fig.15. C2 fault detection probability (Filter 1)

TABLE II
FILTER 1: FAULT COVERAGE

Deviation Fault (% of the nominal value)	*Fault coverage (%)*
-40	99.29
-30	91.63
-20	54.66
+20	39.52
+30	73.11
+40	87.66

2) Filter 2

The fault simulation results are presented following the criteria employed for Filter 1. The results for R_1 are depicted in Fig. 16. It should be mentioned that the *FDP* for deviations in R_2 also exhibit the behavior presented in Fig. 16. For this reason, the referred results are not presented in the paper. The results valid for C_1 and C_2 are reported in Figs. 17 and 18 respectively.

From the above-mentioned figures, it is possible to observe that measurements of both, Tp and OS are required for obtaining good FDP_{ci} for the addressed deviations. In this sense, these measurements are complementary.

For resistors R_1 and R_2, it is possible to observe relatively good FDP_{ci} by means of Tp measurements. Deviations higher than ±30% produce FDP_{ci} near to 90%. Despite this fact, it should be mentioned that small deviations in these components are hard to be detected. We remark the low efficiency of TRAM for detecting deviation in R_1 and R_2, when only OS measurement is implemented.

The *FDP* for deviations in C_1 shows the best performance when OS is monitored. Very good FDP_{ci} are obtained for deviations of ±20%. This is an interesting result showing the test scheme is very sensitive to deviations in the value of this capacitor. However, for C_2 the best performance is obtained when Tp is monitored. It is also observed a high sensitivity to deviations in this capacitor.

The above fault coverage determined for Filter 1 is also calculated for Filter 2 and it is depicted in Table III.

From this table, high fault coverage is obtained for deviation faults of ±30%. In this sense, the performance or TRAM is better for this filter. Additionally, global fault

coverage of 87% is obtained by taking into account deviation faults of ±20% and ±40%.

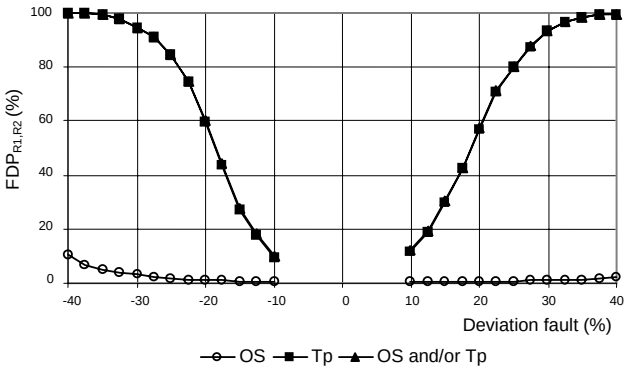

Fig. 16. R_1 and R_2 fault detection probability (Filter 2)

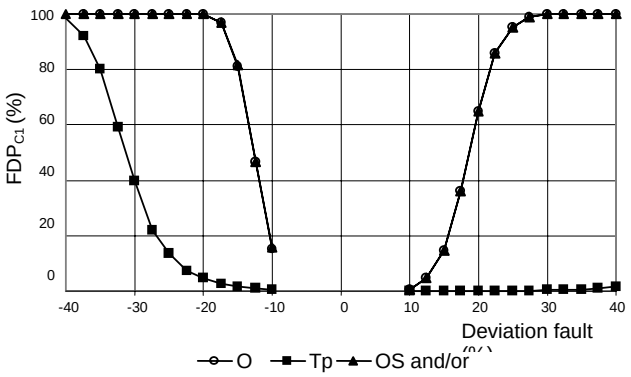

Fig. 17. C_1 fault detection probability (Filter 2)

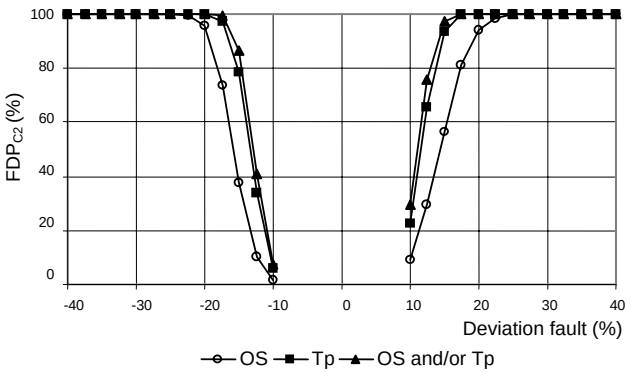

Fig. 18. C_2 fault detection probability (Filter 2)

TABLE III
FILTER 2: FAULT COVERAGE

Deviation Fault (% of the nominal value)	*Fault coverage (%)*
-40	100.00
-30	97.19
-20	80.00
+20	69.88
+30	96.68
+40	99.85

VI. CONCLUSIONS

We present a new performance characterization of TRAM, using more realistic fault models. The ability of the addressed test strategy for detecting deviation faults under simultaneous statistical fluctuation of the non-faulty parameters is evaluated here.

The new data reported in this work for two second-order filters with quite different topologies, adopted as cases of study, show that the Tp and OS measurements are complementary. Consequently, both should be implemented if relatively high coverage is required by the application. This result contrasts with the one obtained by other authors using a simpler fault model. They suggested that only OS measurements are required for obtaining optimal fault coverage. As can be observed from our results, a more complex measurement circuitry is needed and this could complicate the test implementation, especially in BIST schemes.

For Filter 1 it is possible to determine that exist two hard-to-test components and relatively low fault coverage for small deviation faults. Additionally, the global fault coverage is considerable lower than the previously reported ones. For Filter 2, a better performance is obtained, because the fault coverage is relatively low only for deviations faults of 20%. The global fault coverage is higher than the obtained for Filter 1 but considerably departed from the 100% obtained in previous research.

The data reported in this paper show that the application of TRAM should be carefully evaluated by using realistic fault models, because the fault coverage obtained adopting single deviation fault models seem to be poor predictors of the test performance.

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