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New Design Methodologies for High Speed Low Power XOR-XNOR Circuits

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***Abstract*—**New methodologies for XOR-XNOR circuits are proposed to improve the speed and power as these circuits are basic building blocks of many arithmetic circuits. This paper evaluates and compares the performance of various XOR-XNOR circuits. The performance of the XOR-XNOR circuits based on TSMC 0.18µm process models at all range of the supply voltage starting from 0.6V to 3.3V is evaluated by the comparison of the simulation results obtained from HSPICE. Simulation results reveal that the proposed circuit exhibit lower PDP and EDP, more power efficient and faster when compared with best available XOR-XNOR circuits in the literature.

***Keywords*—**Exclusive-OR (XOR), Exclusive-NOR (XNOR), High speed, Low power, Arithmetic Circuits.

I. Introduction

WHILE the growth of the electronics market has driven the VLSI industry towards very high integration density and system on chip designs and beyond few GHz operating frequencies, critical concerns have been arising to the severe increase in power consumption and the need to further reduce it. Moreover, with the explosive growth the demand and popularity of portable electronics is driving designers to strive for smaller silicon area, higher speeds, longer battery life, and more reliability. Power is one of the premium resources a designer tries to save when designing a system. The XOR-XNOR circuits are basic building blocks in various circuit especially-Arithmetic circuits (Full adder, and multipliers), Compressors, Comparators, Parity Checkers, Code converters, Error-detecting or Error-correcting codes, and Phase detector circuit in PLL. The performance of the complex logic circuits is affected by the individual performance of the XOR-XNOR circuits that are included in them [1]-[6]. Therefore, careful design and analysis is required for XOR-XNOR circuits to obtained –full output voltage swing, lesser power consumption and delay in the critical path. Additionally, the design should have a lesser number of transistors to implement XOR-XNOR circuits and simultaneous generation of the two non-skewed outputs.

In this paper a PTL based XOR and XNOR circuits were considers. Despite the saving in transistor count, the output voltage level is degraded at certain input combinations. The reduction in voltage swing, on one hand, is beneficial to power consumption. On the other hand, this may lead to slow switching in the case of cascaded operation. We propose and compare new XOR-XNOR circuit designs which produce the XOR-XNOR outputs simultaneously with full output voltage swing. The NMOS and PMOS transistors are added to the basic circuits to alleviate the threshold voltage loss problem commonly encountered in pass transistor logic design. To overcome the problem of skewed outputs basic XOR-XNOR designs are combined in one circuit.

II. Previous Work

Exclusive–OR and Exclusive-NOR, denoted by $\oplus$ and $\odot$ respectively, are binary operations that perform the following Boolean Functions-

$$x \oplus y = x'y + xy'$$
$$x \odot y = xy + x'y'$$

In the past two decades, a number of circuit techniques have been reported with a view to improve the circuit performance of XOR-XNOR gates [7]-[11]. Albeit it is unusable to include every technique in the literature, in this section we have presented an overview of some significant techniques. A wide variety of XOR-XNOR implementations are available to serve different speed and density requirements. Transistor count and full output voltage swing are, of course, a primary concern that largely affects complexity of many digital functional units.

In [1]-[3], the XOR-XNOR circuits design in static CMOS with complementary pull-up PMOS and pull-down NMOS networks is the most conventional one but it requires more numbers of CMOS transistors. The circuit can operate with full output voltage swing.

Instead of cascading two 2-input XOR gates, a new design for 3-input XOR circuit is given in [4]. The reported circuit has the least number of transistors and no complementary input signals are needed. Especially, the power-delay product is also minimized.

A PTL based 6-transitors XOR and XNOR circuits presented in [6] had full output voltage swing and better driving capability. To compare the performance of new circuit and test their driving capability, an adder circuit is built with

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the proposed XOR and XNOR circuits. An XOR and XNOR function with low circuit complexity can be achieved with only 4 transistors in PTL [7]. Despite the saving in transistor count, the output voltage level is degraded at certain input combinations. A new set of low power 4-transistor XOR and XNOR circuits called powerless (P-) XOR and Groundless (G-) XNOR respectively are proposed in [8]-[9]. The P-XOR and G-XNOR consumes less power than other design because it has no power supply (V_{DD}) or ground (V_{SS}) connection. The Pass-Transistor Logic (PTL) is a better way to implement circuits designed for low power applications. The low power pass transistor logic and its design and analysis procedures were reported in [12]-[14]. The advantage of PTL is that only one PTL network (either NMOS or PMOS) is sufficient to perform the logic operation, which results in smaller number of transistors and smaller input loads, especially when NMOS network is used. Moreover, V_{DD}-to-GND paths, which may lead to short-circuit energy dissipation, are eliminated.

10-transistor circuits for XOR-XNOR function based on transmission gates and inverters were presented in [15]. This circuit can operates at lower supply voltage and have a full output voltage swing for all input combinations. Also, the uses of static CMOS inverters enhance the driving capability at the cost of extra power consumption.

The reported circuit in [16] is consisting of complementary input signals and forward and backward feedback loops. The dual feedback network is used to rectify the degraded logic level problem i.e. forward feedback loop is used to improve the output voltage level for input combinations (00) and (11) while the backward feedback loop is used to enhance the output logic level of the circuit for input combinations (01) and (10). This feedback configuration enhances the circuit performance as well as fan out also. The reported dual feedback network is shown in Fig. 1.

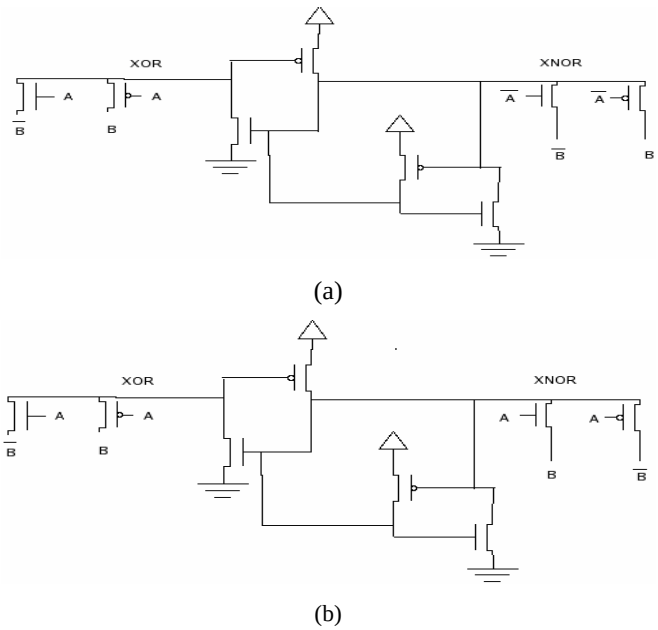

Fig. 1 XOR-XNOR circuits reported in [16]

III. Proposed XOR-XNOR Circuits

The proposed XOR and XNOR circuits are based on the modified version of a CMOS inverter and pass transistor logic. In proposed circuit-I, for XOR when the input B is at logic 1, the inverter circuit functions like a normal CMOS inverter. Therefore, the output is the complement of input A. When the input B is at logic 0, the CMOS inverter output is at high impedance. However, the PMOS pass transistor is ON and the output gets the same logic value as input A. The operation of the whole circuit is thus like a 2-input XOR circuit. However, it performs non full-swing operations for some input patterns causing their corresponding outputs to be degraded by $|V_{th}|$. The proposed XOR-XNOR circuit-I is shown in Fig. 2. The output voltage levels of this circuit for each input combination are shown in Table I.

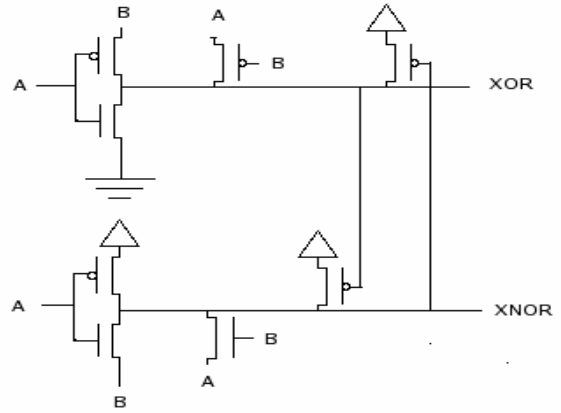

Fig. 2 Proposed XOR-XNOR circuit-I

TABLE I
Input and Output Values for XOR and XNOR Circuits for Fig. 2

Inputs		Outputs	
A	B	XNOR	XOR
0	0	Good 1	Bad 0
0	1	Good 0	Good 1
1	0	Good 0	Bad 1
1	1	Good 1	Good 0

In proposed circuit-II when the input B is at logic 1, the PMOS pass transistor is OFF and NMOS pass transistor is ON. Therefore, the XOR output of the circuit is the complement of input A and XNOR output gets the same logic value as input A. When the input B is at logic 0, the XNOR output of the circuit is the complement of input A and XOR output gets the same logic value as input A for the reason that PMOS pass transistor is ON and NMOS pass transistor is OFF. The cross-coupled two PMOS transistors and two cross-coupled PMOS and NMOS transistors are connected between XOR and XNOR outputs. This arrangement eliminates the non-swing operation. Aspect ratio of the inverter circuit must be high for high driving capabilities. The input and XOR-XNOR output waveforms for the proposed circuit-II are shown in Fig. 3.

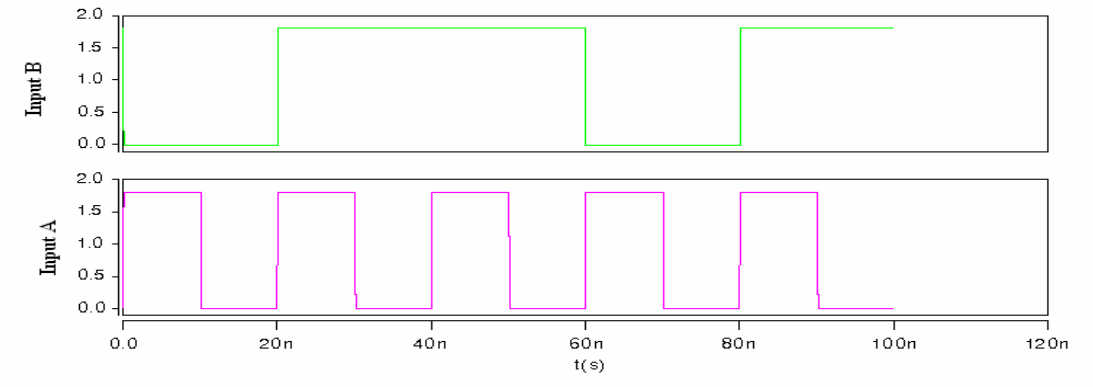

Fig. 3(a) Input waveforms for the proposed circuits

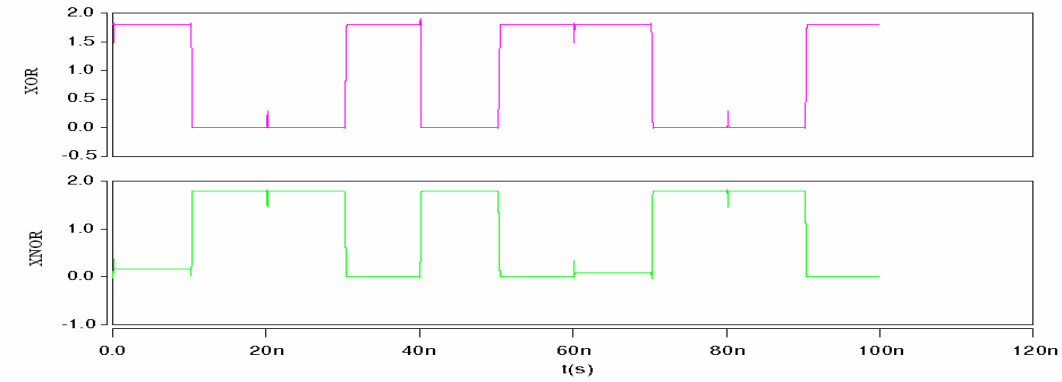

Fig. 3(b) Output waveforms for the proposed circuit-II

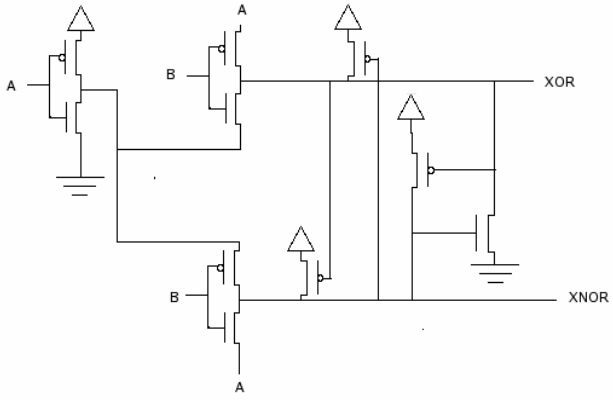

Fig. 4 Proposed XOR-XNOR circuit-II

The proposed XOR-XNOR circuit-II is shown in Fig. 4. The output voltage levels of this circuit for each input combination are shown in Table II.

TABLE II
INPUT AND OUTPUT VALUES FOR XOR AND XNOR CIRCUITS FOR FIG. 4

Inputs		Outputs	
A	B	XNOR	XOR
0	0	Good 1	Good 0
0	1	Good 0	Good 1
1	0	Bad 0	Good 1
1	1	Good 1	Good 0

IV. SIMULATION RESULTS AND COMPARISONS

The transient and DC analyses of the circuits were performed on HSPICE at a supply voltage ranging 0.6V-3.3V using TSMC 0.18µm CMOS process. A constant output load capacitance of 5.6fF is used for power and delay measurements. The simulation test bench used is shown in Fig. 5. Comparison of the worst case delay, power consumption, PDP, and EDP of all designs at the lowest supply voltage of 0.6V of reported and proposed circuits are shown in Fig. 6.

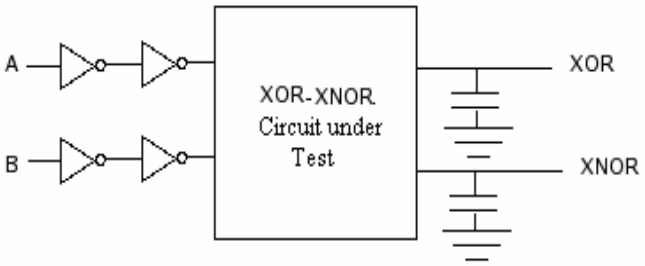

Fig. 5 Simulation test bench

The delay is measured between the time when the changing input reaches its 50% voltage level to the time when the resulting output reaches its 50% voltage level for both rise and fall output transitions. The worst case delay is the largest

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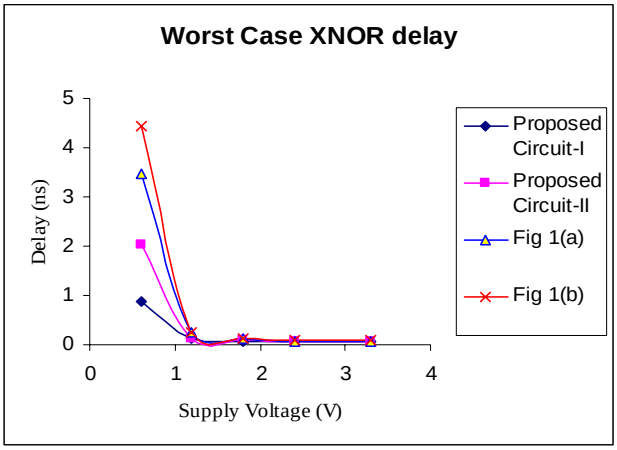

Fig. 6(a) Worst case delay of different XNOR circuits

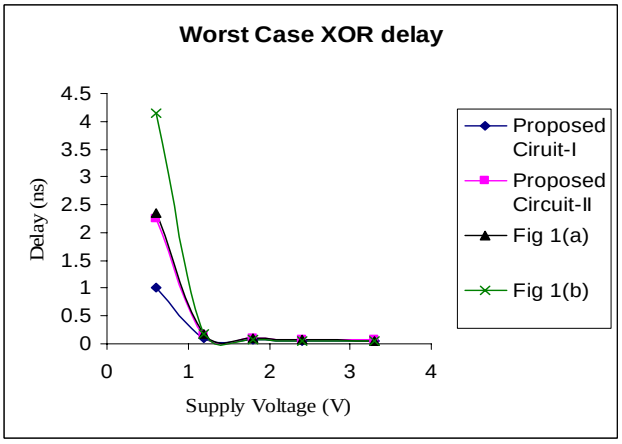

Fig. 6(b) Worst case delay of different XOR circuits

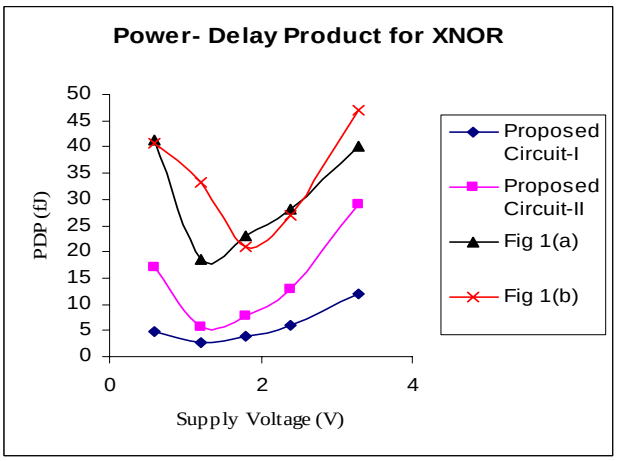

Fig. 6(c) PDP Vs supply voltage graph for different XNOR circuits

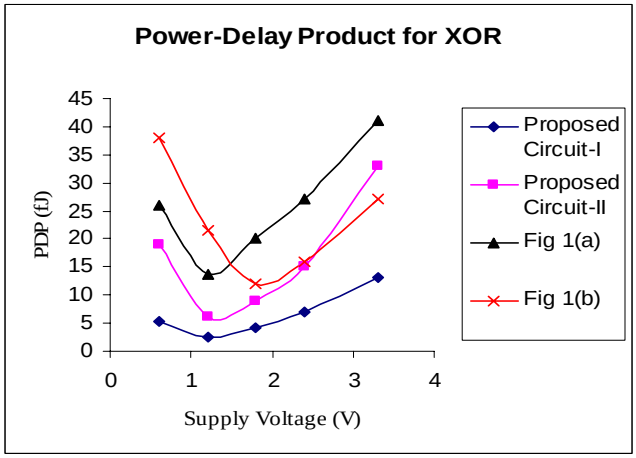

Fig. 6(d) PDP Vs supply voltage graph for different XOR circuits

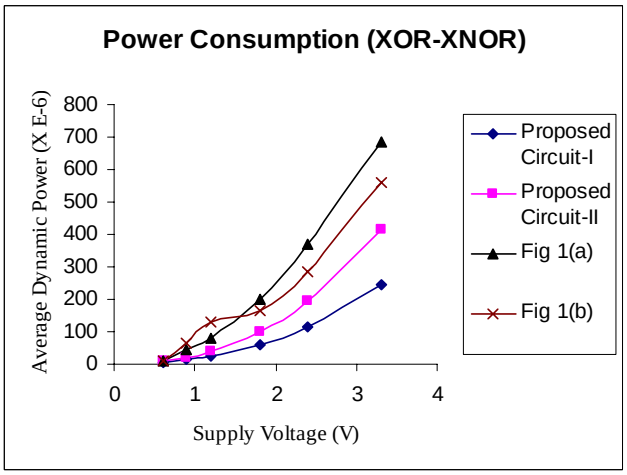

Fig. 6(e) Power Consumption Vs supply voltage graph for different XOR-XNOR circuits

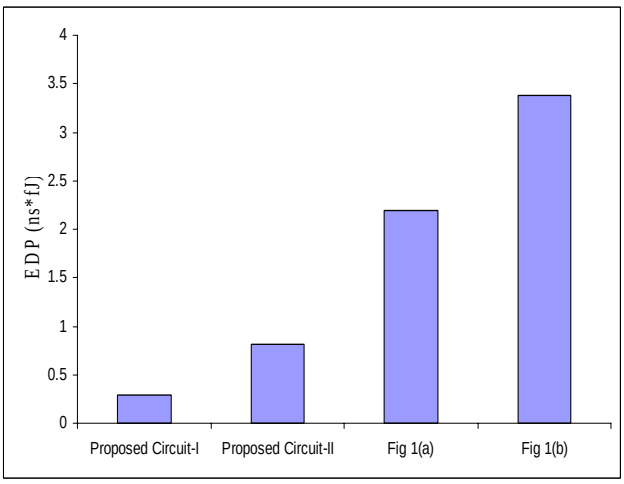

Fig. 6(f) EDP of different XOR-XNOR circuits at 1.8V supply voltage

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delay among all input signals. The proposed circuits give the better performance than the reported circuits in Fig. 1 in terms of worst case XNOR delay. The proposed circuits are 31% to 47% faster than the reported circuits at 1.8V supply voltage. The simulation results of worst case XNOR delay for all circuits are shown in Fig. 6(a).

Compared to the reported circuit in Fig. 1, the worst case XOR delay characteristics of the proposed circuit-I are improved by 4% to 30% at the supply voltage of 1.8V. The proposed circuit-II and Fig. 1(a) shows similar results in terms of worst case XOR delay as shown in Fig. 6(b). Overall, proposed circuit-I shows better worst case XOR delay characteristics.

The power-delay product (PDP) measured in fJ is defined as the product of the worst case delay and the average power consumption. The overall PDP for the proposed circuits have been improved by 53% to 84% at the supply voltage of 1.8V when compared with the reported circuits in Fig.1 as shown in Fig. 6(c) and Fig. 6(d).

The power consumption is measured with the same input settings as for the propagation delay measurement. The simulation results of the average power consumption shown in Fig. 6(e). Subsequently the average dynamic power of proposed circuits is 40% to 64% and 50% to 70% lower than the reported circuits of Fig. 1(a) and Fig. 1(b) respectively.

Energy delay product (EDP) is equal to the product of worst case delay and PDP is reported in Fig 6(f).

Comparison of DC analysis results of different XOR-XNOR circuits are shown in Fig. 7.

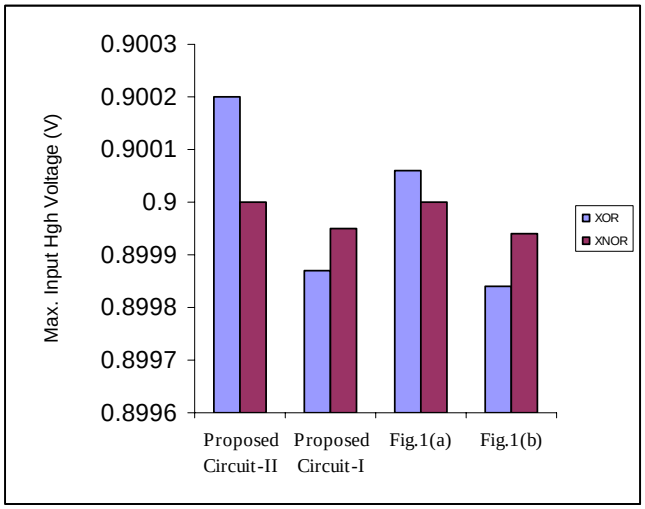

Fig. 7(a) V_{IH} of different XOR-XNOR circuits at 1.8V supply voltage

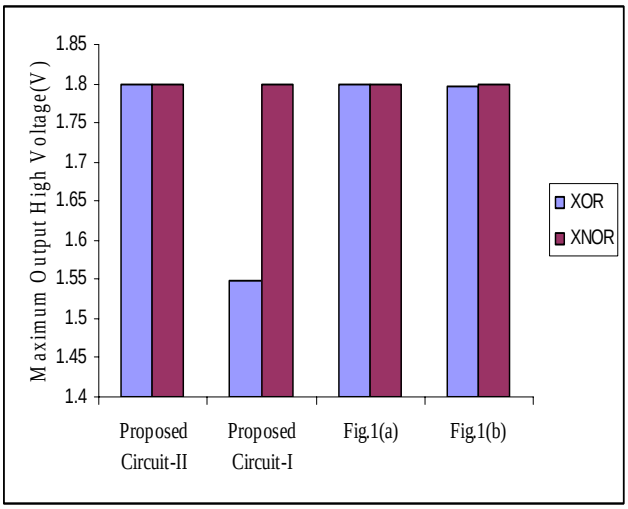

Fig. 7(b) V_{OH} of different XOR-XNOR circuits at 1.8V supply voltage

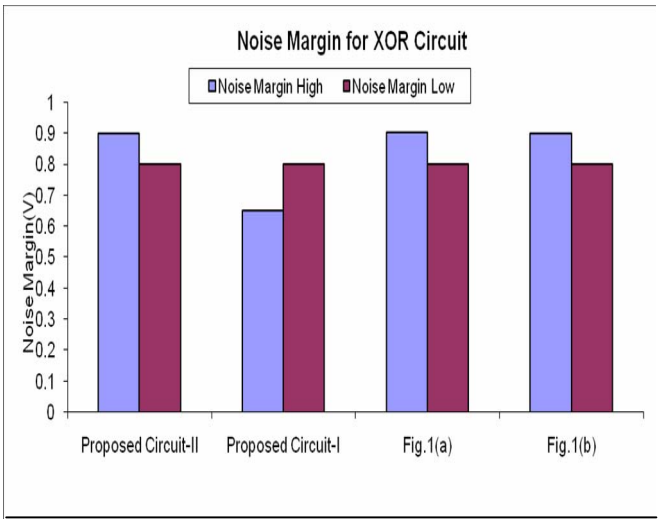

Fig. 7(c) Noise Margin of different XOR circuits at 1.8V supply voltage

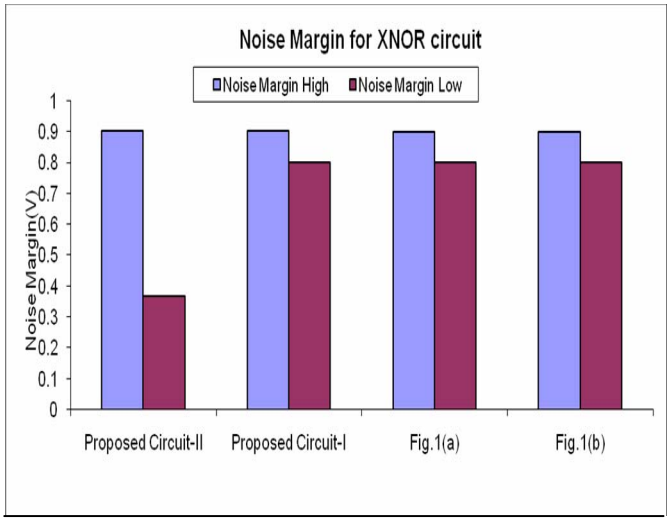

Fig. 7(d) Noise Margin of different XNOR circuits at 1.8V supply voltage

TABLE III
COMPARATIVE PERFORMANCE FOR CIRCUITS IN FIGS. 1, 2, AND 3 AT V_{DD}= 1.8V

	Fig. 1(a)	Fig. 1(b)	Proposed Circuit-I Fig. 2	Proposed Circuit-II Fig. 4
# of transistors	10	12	8	10
Delay XOR (ns)	0.0995	0.0725	0.0695	0.0905
Delay XNOR (ns)	0.1155	0.1295	0.068	0.0795
Average Dynamic Power Consumption (mW)	0.1647	0.2013	0.05859	0.0987
PDP (fJ)	19.02	26.068	4.072	8.93
EDP(fJ*ns)	2.197	3.3758	0.2830	0.8082

Ideally, the difference in V_{IL} and V_{IH} is zero; however, this is never the case in real logic circuits. The input voltage, V_{IL} is approximately 0.8V for all XOR and XNOR circuits.

The performances of XOR-XNOR circuits based on V_{OH} and V_{IH} is shown in Fig. 7(a) and Fig. 7(b), respectively.

The minimum output low voltage V_{OL} is 0V for all XOR circuits and for all XNOR circuits except proposed circuit-II for which V_{OL}=0.4327V.

The noise margin of digital circuits indicates how well the circuit will perform under noisy conditions. The noise margin of the XOR-XNOR circuit in the different methodologies has also been studied. The comparative performance of noise margin of different XOR and XNOR circuits at 1.8V supply voltage is shown in Fig. 7(c) and Fig. 7(d), respectively. The noise margin of the proposed XOR-XNOR circuits indicates quite comparable values with its peer designs. The comparative performance for all circuits at V_{DD} =1.8V are shown in Table III.

V. CONCLUSION

In this paper, we have proposed a new design for XOR-XNOR circuits. The mentioned methodologies based on a delay, power consumption, PDP, and EDP. The performances of these circuits have been evaluated by HSPICE using a TSMC 0.18µm CMOS technology. The proposed circuits are suitable for arithmetic circuits and other VLSI applications with very low power consumption and a very high speed performance. Based on the simulation results, it has been culminated that the new proposed XOR-XNOR circuits have good output signal levels, consume less power and have high speed compared to the previous designs at low supply voltage.

APPENDIX

The transient and DC analyses of the circuits were performed on HSPICE at a supply voltage ranging 0.6V-3.3V using TSMC 0.18µm CMOS process. TSMC 0.18µm SPICE transistor parameter for NMOS and PMOS transistors are given in Table IV. Minimum feature size for TSMC 0.18 µm CMOS process is 0.18 µm and maximum supply voltage (V_{DD}) is 1.8V.

TABLE IV
TSMS 0.18 µM SPICE PROCESS PARAMETER

.MODEL CMOSN NMOS LEVEL=49	
+VTH =0.3770	UO=279.353
+TOX=4.1E-9	XJ=1E-7
+DELTA=0.01	VSAT=1.0837E5
+CJ=9.494E-4	CJSW=2.615E-10
+PB=0.8	CGSO=9.08E-10
+XL=0	XW= -1E-84
+RSH=6.7	ETAO=2.874E-3
+MJ=0.3808	MJSW=0.1054
+CGDO=9.08E-10	CGBO=1E-12
.MODEL CMOSP PMOS LEVEL=49	
+VTH = -0.4001	UO=112.345
+TOX=4.1E-9	XJ=1E-7
+DELTA=0.01	VSAT=1.937E5
+CJ=1.148E-3	CJSW=2.598E-10
+PB=0.8525	CGSO=7.36E-10
+XL=0	XW= -1E-8
+RSH=7.8	ETAO=3.063E-4
+MJ=0.4192	MJSW=0.3335
+CGDO=7.36E-10	CGBO=1E-12

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