World Academy of Science, Engineering and Technology
International Journal of Electrical and Computer Engineering
Vol:2, No:10, 2008

Estimation Of Attenuation And Phase Delay In Driving Voltage Waveform Of An Ultra-High-Speed Image Sensor by Dimensional Analysis

V. T. S. Dao, T. G. Etoh, C. Vo Le, H. D. Nguyen, K. Takehara, T. Akino, K. Nishi

Abstract—We present an explicit expression to estimate driving voltage attenuation through RC networks representation of an ultra-high-speed image sensor. Elmore delay metric for a fundamental RC chain is employed as the first-order approximation. By application of dimensional analysis to SPICE simulation data, we found a simple expression that significantly improves the accuracy of the approximation. Estimation error of the resultant expression for uniform RC networks is less than **2%**. Similarly, another simple closed-form model to estimate 50 % delay through fundamental RC networks is also derived with sufficient accuracy. The framework of this analysis can be extended to address delay or attenuation issues of other VLSI structures.

Keywords—Dimensional Analysis, Elmore model, RC network, Signal Attenuation, Ultra-High-Speed Image Sensor.

I. Introduction

ETOH et al. [1]- [2] developed a CCD image sensor for ultra high speed continuous image capturing. Each pixel of the sensor is equipped with an in-situ storage area with more than one-hundred CCD storage elements. Image signals generated at each pixel are transferred to each storage area and simultaneously recorded at all pixels. This feature enables image capturing at frame rate as high as 1 mega frames/second (Mfps). The sensor was named the ISIS, the In-situ Storage Image.

The design of the ISIS is being continuously improved for much higher frame rate and sensitivity [3]- [4]. One of the most critical factors to achieve the frame rate of 100 Mfps is attenuation of voltage waveforms to drive the CCD, caused by propagation delay. We have to optimize various gates within the ISIS since the one with highest attenuation will define the maximum working frame rate of the sensor.

This paper presents an efficient method to estimate the attenuation due to RC delay of the driving voltage waveform on the sensor chip. We focus exclusively on RC trees that have constant series resistance, parallel resistance and capacitance, a commonly used model in CCD design, as shown later in Fig. 1(b). Elmore delay metric [5] for a fundamental RC chain was utilized as the first-order approximation, and we applied dimensional analysis to circuit simulation data to seek a simple expression to improve the accuracy. Therefore, we call it The Semi-Empirical Interconnect Model (SEIM).

This work is supported by JST, The Japanese Science and Technology Agency.

V. T. S. Dao, T. G. Etoh, C. Vo Le, H. D. Nguyen, K. Takehara are with the Kinki University, Graduate School of Science and Engineering, Higashi-Osaka, 577-8502 Japan; e-mail: vtsdao@ civileng.kindai.ac.jp (corresponding author only).

T. Akino is with the Kinki University, School of Biology-Oriented Science and Technology, Wakayama, 649-6493 Japan.

K. Nishi is with the Kinki University Technical College, Kumano, Mie, 519-4935 Japan.

II. Previous works

A. Delay Computation

Elmore delay metric [5], is the most widely applied interconnect delay metric. Assume an RC tree circuit with n nodes (i = 1, 2, ... , n), and corresponding resistor R_i and grounded capacitor C_i, the Elmore delay at node i is given by:

$$T_{Di} = \sum_{k=1}^{N} R_{ki} C_k \tag{1}$$

where R_{ki} is the resistance of the unique path from input to node i that overlaps with the unique path between node i and node k and C_k is the capacitance at node k.

While the simple expression is useful in practice, Elmore model is known to give low accuracy results due to its first-order moment approximation of the impulse response. To adjust the over-estimation of Elmore model, correction coefficients less than unity have been proposed as listed in [6].

Other approaches have been presented to estimate interconnect delay as follows:

(1) Analytical approach by incorporating the higher order moments of the impulse response, known as model order reduction technique as in [7]- [8]. This approach usually requires intensive computation and is inefficient for physical design and optimization.

(2) Dimensional analysis of simulation results combined with analytical approaches. Dimensional analysis is widely applied to analyses of experimental data to correlate physical parameters governing the phenomena. Dimensional analysis applied to carefully-planned simulation cases is a powerful tool to reach a practical expression, yet, keeping the fundamental importance, especially when combined with analytical approach. Some researches on interconnect delay which utilize this approach as in [6], [9]- [10].

B. Signal Attenuation Computation

There are a lot of researches on delay calculation for a step excitation or ramp excitation as listed in [5]- [12], but not much work has been done for cases, e.g. input signal is periodic clock (pulse train type) in which the frequency effect

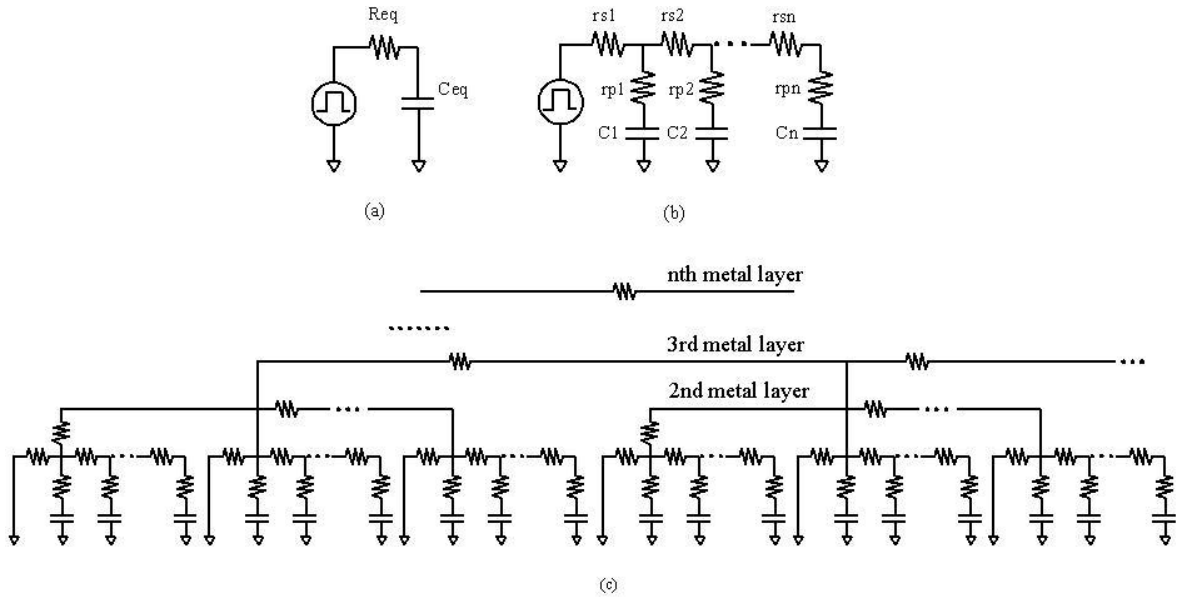

Fig. 1. Circuit structure (a) Equivalent RC circuit (b) Fundamental RC circuit (c) Multi-level RC circuit.

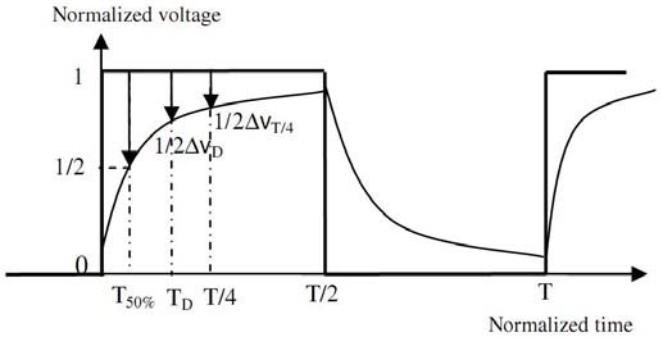

Fig. 2. Input-output waveform pair; $\frac{\Delta V_D}{2}$, $\frac{\Delta V_{T/4}}{2}$: half (one-side) signal loss calculated at T_D and quarter cycle (T/4)..

of the input signal must be taken into account when building models. Celik and Pillegi [12] approximately estimate the amplitude response by using a function of the fundamental frequency of the input signal and the second central moment of circuit parameters.

III. BACKGROUND ON CURRENT WORK

A. Multi-level structure of the ISIS

CCD structure is usually represented with a multi-level model of the fundamental structure as shown in Fig. 1(c). Interconnect capacitance is neglected, since capacitance of polysilicon gate is dominant for CCD. We can adjust the total capacitance later by introducing a correction factor. Therefore, it is safe to use the model in Fig. 1(b) for evaluation of propagation delay of CCD structure. Fig. 1(b) shows a fundamental RC chain circuit with series resistance r_S, parallel resistance r_P and grounded capacitor c. The fundamental model can be replaced with some allowance of accuracy by the electrically-equivalent simplest model with equivalent resistance R_{eq} and capacitor C_{eq} as shown in Fig. 1(a). Similar steps are repeated depending on the number of metal layers of the ISIS. The final equivalent resistance and capacitance are used to balance the RC delay.

Interconnect model derived in this paper is based on the following assumptions:

(1) Uniformly distributed RC networks in Fig. 1(b) with constant r_S, r_P and c;

(2) Square input waveform - duty cycle is 50%, which is normally used in high speed four-phase CCD transfer;

(3) Performance evaluation is based on amplitude response of the furthest-end node.

B. Attenuation approach for fundamental RC chains

For RC circuits with monotonic responses as shown in Fig. 2, we always have:$0.5 \geq \Delta V_D/2 \geq \Delta V_{T/4}/2$. Therefore, we can conclude that Elmore model still can be used as the upper bound for attenuation estimation or lower bound for amplitude response estimation. We will focus to find a proper correction factor for Elmore model in this paper.

C. Dimensional analysis

We have seven factors involved in evaluating amplitude loss from a fundamental RC chain as in Fig. 1(b) and Fig. 2:

- parallel resistance r_P,
- series resistance r_S,
- grounded capacitance c,
- clock period T,
- input amplitude V_0,
- amplitude loss at quarter cycle $\Delta V_{T/4}$,
- number of sub-circuit segments n.

To reduce the number of governing parameters of the system and derive a generalized expression for the RC delay,

TABLE I
ATTENUATION VERSUS B FOR A SINGLE RC CIRCUIT

B	0.001	0.01	0.02	0.04	0.055
$\overline{\Delta V}_{T/4}/2$	3E-109	1.4E-11	4E-6	0.002	0.0106
B	0.08	0.11	0.13	0.165	0.18
$\overline{\Delta V}_{T/4}/2$	0.044	0.1030	0.1462	0.2203	0.2494

parameters selected as "base" parameters are: n, r_S, r_P, c and T.

Then, the following three dimensionless parameters are introduced:

(1) Dimensionless amplitude loss at quarter cycle:

$$\overline{\Delta V}_{T/4} = \Delta V_{T/4}/V_0 \tag{2}$$

(2) Ratio of equivalent parallel resistance and series resistance:

$$A = \frac{R_P}{R_S} = \frac{2}{n(n+1)}\frac{r_P}{r_S} \tag{3}$$

(3) Ratio of the first-order approximation of RC delay (Elmore model) and pulse period:

$$B = R_E C_E f \tag{4}$$

where f is the driving pulse frequency.

Thus, dimensional analysis results in the following dimensionless equation:

$$\Phi(\overline{\Delta V}, A, B) = 0 \tag{5}$$

While an explicit expression is more useful, we focus on finding the function:

$$\overline{\Delta V} = \Phi_1(A, B) \tag{6}$$

The functional relationship in equation (6) can be estimated through an equivalent circuit with the resistance R_{eq} and the capacitance C_{eq}, where: $C_{eq} = C_E = nc$.

The expression of Req is assumed as follows:

$$R_{eq} = \alpha(R_P + \beta R_S) \tag{7}$$

Then, our problem is reduced to obtain an expression of α and β in terms of dimensionless parameters A and B. They were determined experimentally by using a practical procedure described in Section IV.

D. Practical range of attenuation

Theoretically, B can vary from 0 to ∞. However, if B is too small, attenuation becomes almost negligible, and if B is too large, signal becomes completely attenuated; both cases are of no interest for practical applications. Therefore, the range of B is fixed between **0.055** and **0.18** which corresponds to the one-side attenuation of **1%** and **25%** of input voltage amplitude of a single RC circuit shown in Fig. 1(a) and Table I.

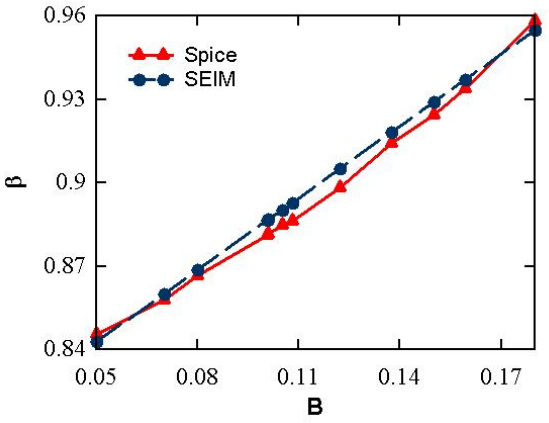

Fig. 3. β fitting result when $A = 0$.

IV. SEMI-EMPIRICAL INTERCONNECT MODEL (SEIM)

A. Two extreme cases (A = ∞ or A = 0)

For $A = \infty (r_S = 0)$, we have an analytical solution: $R_{eq} = R_P = r_P/n; C_{eq} = nc$. Therefore, $\alpha = 1$. For A = 0 ($r_P = 0$), hence, $r_P = 0$, and from equation (7), we have: $R_{eq} = \alpha\beta R_S$. We can expect that the value of α distributes around unity, which is the exact solution for $A = \infty$. It is convenient for the following analysis if α can be fixed at a constant. Therefore, α is assumed to be one. Then, we searched for an expression of β with respect to B.

The coefficients were found by applying a curve fitting technique to fit SPICE data with a wide range of number of circuit segments (n) from 10 to 20,000 with different B. The result of β is as follows:

$$\beta = 0.86B + 0.8; 0.055 \le B \le 0.22 \tag{8}$$

Fig. 3 shows an excellent linear fitting result between SEIM and Spice data with less than 0.7% for A = 0 and $\alpha = 1$.

B. General cases in which $A \neq \infty$ and $A \neq 0$

The two simple cases examined above are used as "boundary conditions" to find the functional relationship for the whole range of A. For the general cases of A which distributes from 0 to ∞, we assume that expression of β with respect to B remains unchanged, and α changes with respect to A.

We employed the following expression to approximate the change of α with respect to A for $0 \le A \le \infty$:

$$\alpha(A) = 1 + aA^b e^{-cA}; a = a(B); b = b(B); c = c(B) \tag{9}$$

The coefficients a, b and c in equation (9) were found by using Powell conjugate minimization technique to fit SPICE data with a wide range of circuit at different combinations of (n, r_S, r_P, c and f) for different cases of B as shown in Fig. 4. Finally, we have a simple functional form of SEIM as

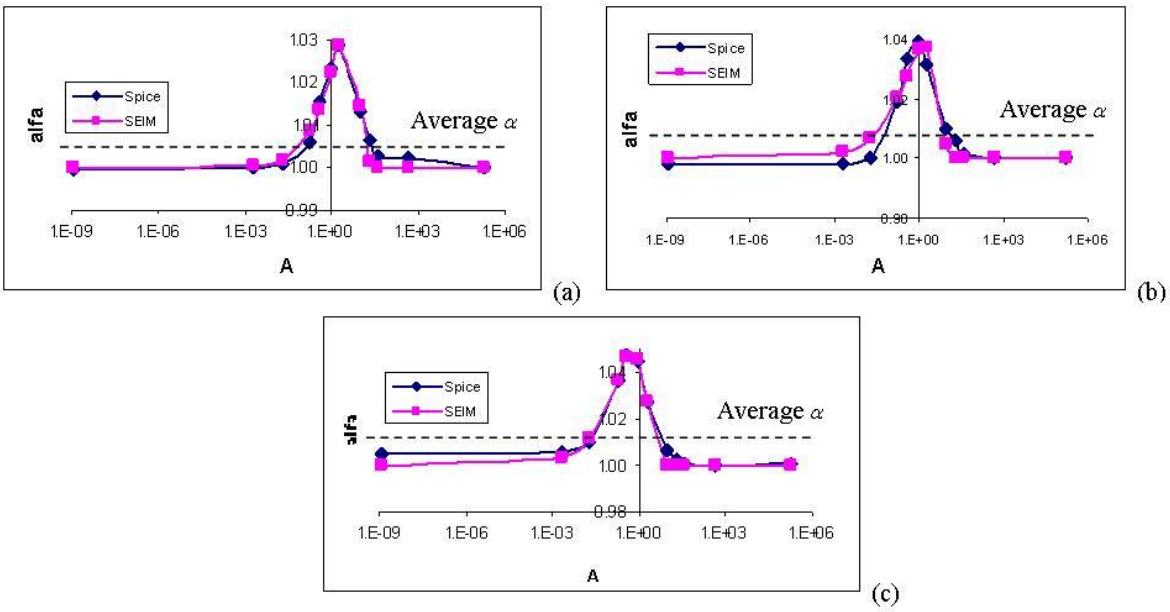

Fig. 4. α fitting result when B = 0.055(a); 0.11(b); 0.165(c) and 0.22(d).

follows:

$$\begin{aligned} R_{SEIM} &= \alpha(R_P + \beta R_S); \\ \beta = 0.86B + 0.8; &\alpha = 1 + aA^b e^{-cA}; \\ a = 0.67B; &b = -3B + 0.8; \\ c &= 7.42B - 0.3; \\ \text{where: } 0.055 \leq B &\leq 0.22; \end{aligned} \tag{10}$$

Since α changes around unity as shown in Fig. 4, we can further simplify its expression by using the average values of α for each case of B. The Simplified - Semi Empirical Interconnect Model (S-SEIM) is as follows:

$$\begin{aligned} R_{S-SEIM} &= \alpha(R_P + \beta R_S); \\ \beta = 0.86B + 0.8; &\alpha = 0.34B^2 + 0.0047B + 1; \\ \text{where: } 0.055 \leq B &\leq 0.22 \end{aligned} \tag{11}$$

Estimation errors of amplitude response of various testing cases using S-SEIM, SEIM, Elmore [5] and Celik [12] models are shown in Table II. SEIM and S-SEIM give much better results compared with other models in wide range of B.

V. ACCUMULATION ERROR OF MULTI-LEVEL CIRCUIT STRUCTURE

There's a possibility that estimation error accumulates through successive equivalence steps from multi-level circuit structure as in Fig. 1(c) to the final equivalent RC circuit as in Fig. 1(a). We tested the effect of accumulating of error of an example three-level model (20x20x20) with circuit parameters similar to those of an existing ISIS. Equivalent resistance and capacitance of the lower level were used as input data

TABLE II
COMPARISON BETWEEN ESTIMATION ERRORS OF AMPLITUDE RESPONSE BY DIFFERENT MODELS

n	B	Elmore	Celik	SEIM	S-SEIM
5880	0.117	-6.6%	-17%	-0.5%	-0.6%
1280	0.150	-7.6%	-49.5%	-0.9%	-1.2%
720	0.056	-1.3%	-5.5%	0.0%	0.0%
360	0.133	-7.9%	-26.9%	-0.7%	-1.2%
144	0.076	-1.6%	-5.6%	0.2%	0.8%
90	0.1	-2.9%	-9.6%	0.4%	1.2%

for the higher layer circuit. Amplitude response of the final single RC circuits is compared with SPICE simulation data. Experiment result shows that SEIM yields sufficiently small estimation error,**1.4%** , in comparison with **17.0 %** of Elmore model. We can see that the more metal layers the IC has, the more estimation error accumulates. SEIM is served as a much better tool for general optimization purpose in the design flow and give more accurate estimation result without the need of intensive computation effort.

VI. APPLICATION OF SEIM FOR DELAY CALCULATION

In order to prove the effectiveness of SEIM frame work, we derived the closed form expression to estimate propagation delay of clock signal through fundamental RC chain representation of the ultra-high-speed image sensor, ISIS.

A. Two extreme cases ($A = \infty$ or $A = 0$)

Similarly, for $A = \infty (r_S = 0)$, we also have an exact solution: $R_{eq} = R_P = r_P/n, C_{eq} = nc$. Therefore, $\alpha = 1$. For A = 0 ($r_P = 0$), hence, $r_P = 0$, and from equation (7), we have: $R_{eq} = \alpha\beta R_S$. We need to derive delay estimation expression for ladder networks. By constructing $\beta - B$ curve

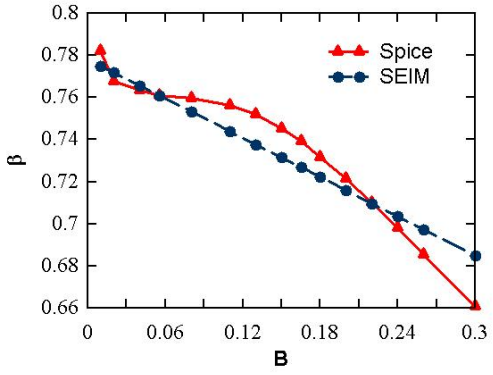

Fig. 5. β fitting result with delay approach.

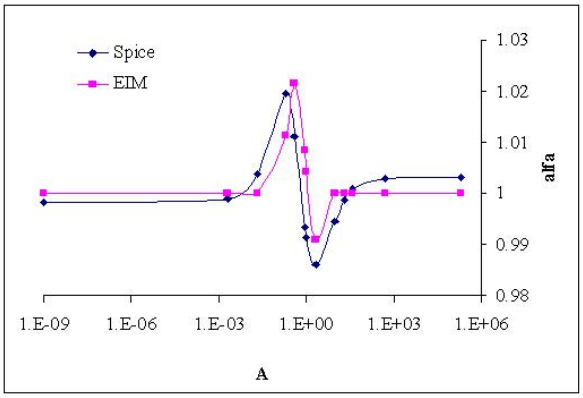

Fig. 6. α fitting result when B = 0.055

with various testing cases of ladder circuits, we found the resultant expression as follows:

$$\beta = 0.31B + 0.78 \tag{12}$$

Expression of β in equation (12) is also consistent with the work of Vlach et al. [11]. They showed that ratio of Elmore delay to SPICE delay for the furthest-end node of RC ladder networks has an average value of **0.7533** with standard deviation of **0.0229**. However, they did not explain the changing behavior of β with respect to circuit parameters. With SEIM, we explained behavior of this ratio in a more systematic way based on the dimensionless parameter B.

B. General cases in which $A \neq 0$ and $A \neq \infty$)

When $0 < A < \infty$, we employed the following expression to approximate the change of α with respect to A as follows:

$$\alpha(A) = abA^{b-1}e^{-cA}(1 - A\frac{c}{b}) + 1 \tag{13}$$

Although delay estimated using equation (13) fits well with SPICE as shown in Fig. 6, the expression of α is more complicated than that in previous case of amplitude response. Instead, we use S-SEIM approach by using a constant value of α for each case of B, and use a quadratic function to estimate α as follows.

TABLE III
DELAY ESTIMATION ERROR FOR FUNDAMENTAL RC CHAINS

B	Elmore	Wyatt($0.69T_D$)	D2M	S-SEIM
0.05	49.1%	3.5%	0.7%	5.3%
0.075	50.1%	4.2%	3.2%	3.1%
0.1	51.5%	5.0%	7.5%	0.1%
0.125	52.7%	6.0%	8.6%	-1.1%
0.154	55%	7.6%	11.6%	-2.7%
0.18	58.1%	9.8%	13.4%	-3.6%

$$\beta = -0.31B + 0.78; \alpha = -2.4B^2 + 0.15B + 1; \quad \text{where: } 0.055 \leq B \leq 0.22 \tag{14}$$

Various testing cases had been used to show the effectiveness of our proposed method. Estimation results by different delay model were summarized and tabulated in Table III Table III shows that S-SEIM gave reasonable delay estimation results than other models even with simplified expression.

VII. Conclusion

Explicit closed-form expressions to estimate driving voltage attenuation and 50% delay of RC networks of an ultra-high-speed image sensor, have been developed. The proposed approach starts from utilizing Elmore model for a fundamental RC chain as the first-order approximation. Then, we applied dimensional analysis to circuit simulator data to seek a simple expression that significantly improve the accuracy of Elmore model. Different fundamental RC chains have been considered and simulated demonstrating the accuracy of the proposed model with respect to Elmore model and Celik model. With simple closed-form type, SEIM can be used effectively in optimization process of metal wiring network of the ultra-high-speed image sensor. Finally, it is worth noting that the proposed approach could be extended to address delay or attenuation of other VLSI structure with different input conditions rather than square input waveform with no input rise time.

References

[1] T. G. Etoh, D. Poggermann, A. Ruckelshausen, A. J. P. Theuwissen, G. Kreider, H. O. Folkerts, H. Mutoh, Y. Kondo, H. Maruno, K. Takubo, H. Soya, K. Takehara, T. Okinaka, Y. Takano, T. Reisinger, and C. Lohman, "A CCD image sensor of 1Mframes/s for continuous image capturing of 103 frames", Digest of Technical Papers, IEEE Int. Solid-State Circuits Conf., San Francisco, CA, pp. 46-47, 2002.

[2] T. G. Etoh, D. Poggermann, G. Kreider, H. Mutoh, A. J. P. Theuwissen, A. Ruckelshausen, Y. Kondo, H. Maruno, K. Takubo, H. Soya, K. Takehara, T. Okinaka, and Y. Takano, "An image sensor which captures 100 consecutive frames at 1,000,000 frame/s", IEEE Trans.Electron Dev., vol. 50, no. 1, Jan. 2003, pp. 144-151.

[3] T. G. Etoh, C. Vo Le, Y. Hashishin, N. Otsuka, K. Takehara, H. Ohtake, T. Hayashida, and H. Maruyama, "Evolution of ultra-high-speed CCD imagers", Plasma and Fusion Research, 2, S1021, 2007.

[4] P. Karimov, , C. Vo Le, K. Takehara, S. Yokoi, and T. G. Etoh, "Photo-triggering system for an ultra high speed video microscopy", Review of scientific instruments, vol.78, 113702, Nov. 2007.

[5] W.C. Elmore, "The transient response of damped linear networks with particular regard to wide-band amplifiers," J. Appl. Phys., vol. 19, no. 1, Jan. 1948, pp. 55-63.

[6] S. Y. Kim and S. S. Wong, "Closed-form RC and RLC delay models considering input rise time," IEEE Trans.Circuits Syst.-I, Regular Papers, vol. 54, no. 9, Sep. 2007, pp. 2001-2010.
[7] L.T. Pillage and R.A. Rohrer, "Asymptotic waveform evaluation for timing analysis," IEEE Trans. Comput-Aided Des.Integr.Circuits Syst., vol. 9, no. 4, Apr. 1990, pp. 352-366.
[8] C. L. Ratzlaff, N. Gopal, and L. T. Pillage, "RICE: Rapid interconnect circuit evaluator," in Proc. IEEE/ACM Design Automation Conf., 1991, pp. 555-560.
[9] Y. I. Ismail and C. Amin, "Computation of Signal Threshold Crossing Times Directly from Higher Order Moments", IEEE Trans. Comput-Aided Des.Integr. Circuits Syst.,vol. 23, no. 8, Aug. 2004, pp. 1264-1276.
[10] D. E. Khalil, Y. Ismail, M. Khellah, T. Karnik, and V. De, "Analytical Model for the Propagation Delay of Through Silicon Vias", in Proc. 9th Int. Symp. Quality Electronic Design, 2008, pp. 553-556.
[11] J. Vlach, J. A. Barby, A. Vannelli, T. Talkhan, and C. J. Shi, "Group delay as an estimate of delay in logic," IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst., vol.10, no. 7, July 1991, pp. 949-953.
[12] M. Celik and L. T. Pillegi., "Metrics and bound for phase delay and signal attenuation in RC(L) clock trees," IEEE Trans.Comput.-Aided Des. Integr. Circuits Syst., vol.18, no. 3, Mar. 1999, pp. 293-300.