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Vertical GAA Silicon Nanowire Transistor with Impact of Temperature on Device Parameters

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***Abstract*—**In this paper, we present a vertical wire NMOS device fabricated using CMOS compatible processes. The impact of temperature on various device parameters is investigated in view of usual increase in surrounding temperature with device density.

***Keywords*—**Gate-all-around, temperature dependence, silicon nanowire

I. Introduction

WITH conventional planar CMOS transistors reaching scaling limits, new device architectures are being investigated [1]. Gate-All-Around (GAA) transistors are reported to have highest scaling potential with channel body reduced to nanometer scale, called as nanowire channel [2]. In vertical format, while enjoying the similar performance with excellent electrostatic control, the GAA wire devices boasts exciting opportunities of space reduction. Interestingly, the vertical wire devices can be fabricated on bulk silicon wafers and thus save the wafer cost in comparison to lateral wire devices which usually require SOI wafers. Further density benefits from vertical wire devices could be through vertical stacking – more than one transistor per wire [3].

Nanowires are fabricated mainly by two general approaches: bottom-up approach and top-down approach. The former provides high density tall narrow nanowires, but the random location growth nature makes it non-ideal for sophisticated circuit use. The latter employs high-end lithography methods to define nanowire arrays directly for circuit-use. This translates to potential feasibility in transferring the technology to large-scale fabrication usage.

In this paper, vertical GAA silicon nanowire transistors are fabricated using the top-down approach, with good controls on wire diameter and gate length. Excellent performance such as high ON current, Low OFF current, Low DIBL and near ideal SS are demonstrated for a device with wire diameter about 40 nm and channel length of 150 nm. Furthermore, the temperature dependence of the device parameters is investigated.

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II. Device Fabrication and Characterization

The vertical GAA silicon nanowire transistors were fabricated on bulk silicon wafers. Shown in Fig.1 is the process flow through schematics. Starting with the deposition of silicon nitride as hard-mask, circular resist patterns, as small as 160nm, were patterned on the hard mask layer. The resist dots were subsequently trimmed by dry-etch to 100nm. The nitride hard mask was etched using plasma dry-etch, followed by etching the underlying silicon, also with dry-etch. Si etch depth defines the height of the nanowire. The silicon pillar was oxidized at high temperature to further reduce the diameter of the silicon core. The oxide is later removed by wet etch, leaving a vertical 40nm diameter silicon nanowire. Gate to source isolation is formed by deposition and etch back of HDP oxide as shown in Fig. 1(a). 45Å gate oxide is grown, followed by deposition of 50nm LPCVD amorphous silicon in Fig. 1(b). Fig. 1(c) shows the remaining HDP oxide after deposition and etch back to expose the top cap of the amorphous silicon. By controlling the etching time of the silicon top cap, the gate length is defined. In this experiment, the gate length was defined to be 150nm.

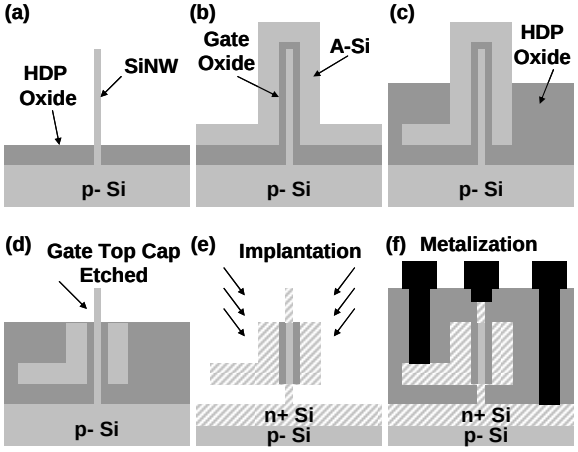

Fig. 1 (a) Si-Nanowire formation with gate-to-source isolation oxide, (b) Gate stack deposition. (c) Gate top cap exposure. (d) Gate top cap etch. (e) Implantation. (f) Contac hole formation and Metallization

In Fig. 1(d), the top cap is removed by selective dry-etch and followed by implantation in Fig. 1(e). The implant energy, dose, and direction is critical to define the junction as close to the silicon nanowire core as possible. Therefore, a four-directional 45 degree tile implant angle is used to ensure the nanowire is symmetrically implanted. Rapid thermal annealing was performed to activate dopants and that was

followed by standard metallization methods, as shown in Fig. 1(f). Some of the critical fabrication processes were captured by tilted top view SEM images. Shown in Fig. 2(a) is the silicon nanowire after thinning by oxidation and subsequently removing the hard mask and oxide. Fig. 2(b) shows the gate stack depositions followed by gate definition and etch, while Fig. 2(c) shows the top gate cap after dry-etch to expose the silicon nanowire top.

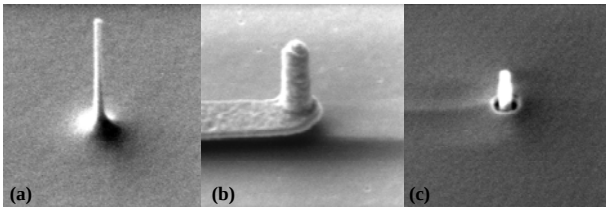

Fig. 2 (a) Single silicon nanowire, (b) Gate stack deposition and gate definition (gate oxide ~50A and gate length 150 nm), (c) Gate top cap etch, for implanting top of nanowire and taking drain contact.

III. Results and Discussion

The fabricated GAA silicon nanowire NMOS were characterized for current-voltage characteristics at various temperatures from room temperature to 95°C. Fig. 3 shows the measured drain current as a function of the gate voltage at V_{DS} = 0.05 and 1.2V at two different temperatures. Device shows excellent turn ON with near ideal SS (~65mV/dec), and very little DIBL. OFF current is in sub-pico ampere regime with ON/OFF ratio about 10^6. All these show that the device structure very suitable for low power applications. With increase in temperature, slight increase in SS and decrease in V_{TH} is visible from the graph. More details analysis of which and comparison with conventional devices is presented later.

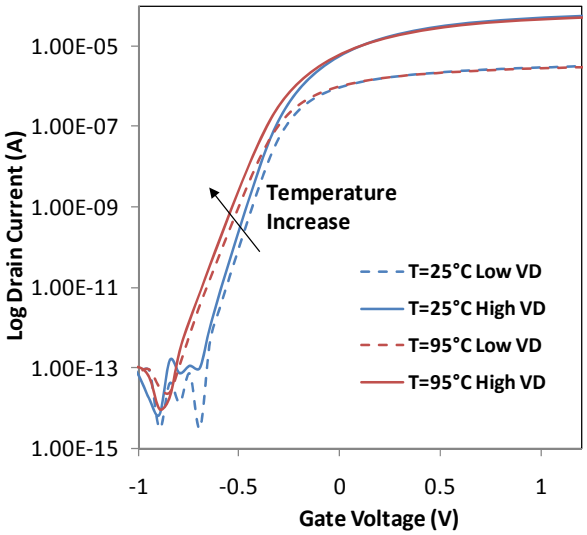

Fig. 3 Measured I_D-V_G characteristics of a Si nanowire GAA NMOS at T=25°C and 95°C, at V_D=+0.05V and +1.2V. Wire diameter ~40 nm and gate length 150 nm, gate oxide thickness ~ 45A.

Shown in Fig. 4 are the Id-Vg characteristics at V_{DS} = V_{DD} of the same device at a step of 10°C from 25°C to 95°C. A systematic decrease in VTH and increase in SS is visible as expected.

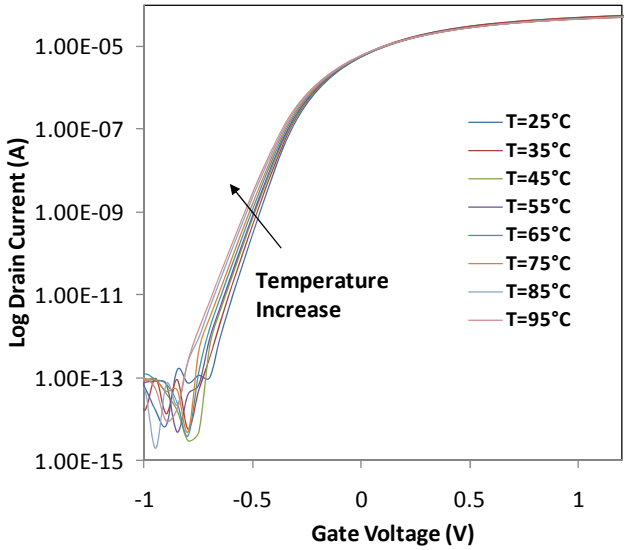

Fig. 4 Measured I_D-V_G characteristics when temperature is gradually increased from 25°C to 95°C with V_D set at +1.2V.

Next, we analyze the impact of temperature on various device parameters. Impact on VTH is presented first. The threshold voltage at T=25°C is extracted by linear extrapolation method [4] and is found comparable to that mentioned in [5]. This extracted threshold voltage is then taken as reference for monitoring threshold voltage shift due to temperature increase.

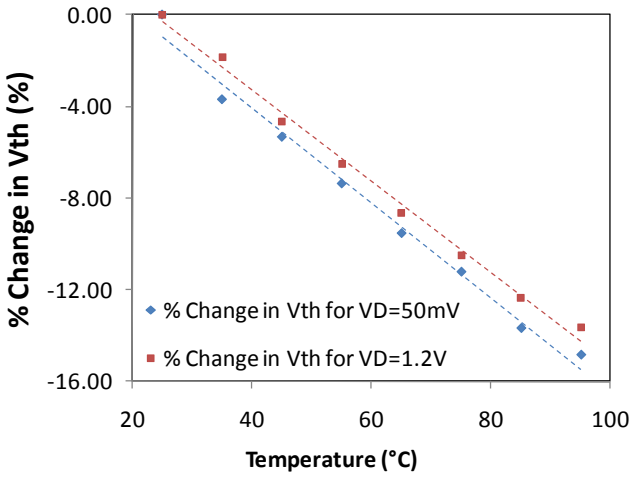

Fig. 5 Percentage change in threshold voltage with respect to temperature change. Negative percentage change in threshold voltage represents an actual decrease in threshold voltage.

Fig. 5 shows the behavior of the threshold voltage change as temperature is increased from T=25°C to T=95°C. The negative percentage change refers to an actual decrease in the threshold voltage as temperature is increased. The behavior is linear as expected from threshold voltage model. The rate of change in threshold voltage when V_D=50mV is -0.63mV/K, which is higher than compared to -0.37mV/K reported in [6] for

3 nm diameter nanowire device. This is due to the difference in diameter of the nanowire, with 50nm reported in this paper and 3nm in the reported literature. Our reported threshold sensitivity is lower than tri-gate device (1.65mV/K) [7] with Fin crossection larger than our wire. So result is in agreement that body size reduction reduces the temperature sensitivity. Rate of change in threshold voltage when V_D=1.2V is found to be -0.67mV/K – both are nearly the same. Shown in Fig. 6 is the effect of temperature on DIBL. No observable difference is noticed as expected.

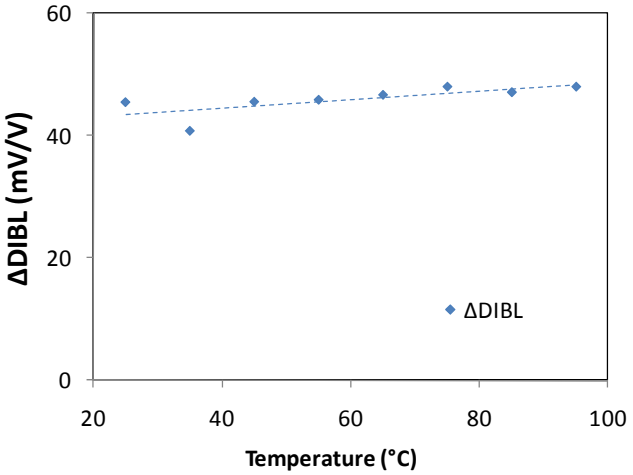

Fig. 6 Variation of DIBL with temperature shows generally a slight increase in DIBL phenomenon, due to a faster rate of change in threshold voltage at higher V_D.

The impact of temperature on measured SS along with ideal value [ln(10)K_BT/q] is presented in Fig. 7. Minor differences between both lines show the ideal turn ON of the vertical GAA silicon nanowire transistor. A little increase in the non-ideality with temperature is observed and being investigated.

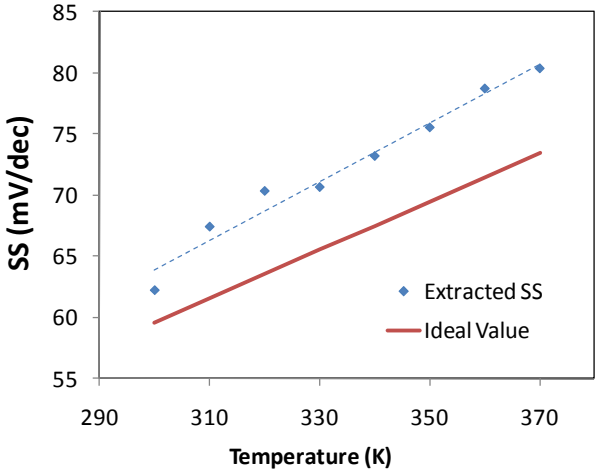

Fig. 7 Plot of both experimental and ideal SS variation with temperature.

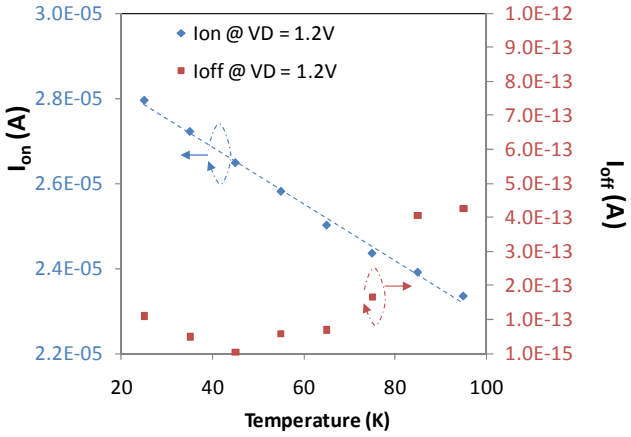

Fig. 8 On/off currents variation with temperature.

Next, the impact of temperature on ON and OFF currents is presented in Fig. 8. As the device threshold was not tuned, we used the method presented by R. Chau, *et al.* [8] in which OFF current is taken at $V_{GS}=V_{TH}-V_{DD}/3$ and ON current at $V_{GS}=.V_{TH}+2V_{DD}/3$. A clear decrease in the ON current is observed due to decrease in mobility attributed to lattice vibrations. Off-current has just random fluctuations and attributable mostly to noise.

IV. Conclusion

In conclusion, a vertical GAA silicon nanowire transistor was presented with temperature studies on the electrical performance. Whilst having superior transistor properties at room temperature, the vertical GAA nanowire transistor has managed to maintain many of these properties even as temperature is increased. This would enhance the cause for integration of vertical GAA transistors into highly dense circuitry.

Acknowledgment

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