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Low Voltage Squarer Using Floating Gate MOSFETs

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Abstract—A new low-voltage floating gate MOSFET (FGMOS) based squarer using square law characteristic of the FGMOS is proposed in this paper. The major advantages of the squarer are simplicity, rail-to-rail input dynamic range, low total harmonic distortion, and low power consumption. The proposed circuit is biased without body effect. The circuit is designed and simulated using SPICE in 0.25μm CMOS technology. The squarer is operated at the supply voltages of $\pm 0.75V$. The total harmonic distortion (THD) for the input signal 0.75Vpp at 25 KHz, and maximum power consumption were found to be less than 1% and 319μW respectively.

Keywords—Analog signal processing, floating gate MOSFETs, low-voltage, Spice, squarer.

I. Introduction

LOW power consumption increases the battery lifetime and the reliability of the portable systems. The most efficient method to reduce the power consumption is lowering the supply voltage because power is directly proportional to the square of the supply voltage. A voltage squarer is a useful non-linear building block [1]-[4] in various circuits such as multipliers, modulators, phase comparators, etc. This paper suggests a new squarer circuit based on FGMOS transistors and shows how FGMOS transistors can be used to reduce the threshold voltage requirement to get rail-to-rail input dynamic range and low power/ low voltage operation. Floating gate MOSFETs have been used to design digital-to-analog (D/A) and analog-to-digital (A/D) converter [5], voltage-controlled resistors [6]-[8], electronic programming [9], neural networks [10], operational transconductance amplifier [11], multipliers [12]-[17], attenuator [16], and squarers [15]-[17]. The squarer proposed in this paper is expected to be useful in the area of low-voltage analog signal processing applications. The analysis of the second order effects such as channel length modulation and mobility degradation show that they have little influence on the proposed circuit. The paper is organized as follows: the operation of the FGMOS is discussed in section II. In section III, the squarer using FGMOS is proposed. A detailed analysis of the channel length modulation and mobility degradation on the performance of the proposed squarer circuit is presented in section IV. In section V, SPICE simulation results are presented to verify the theoretical analysis and to demonstrate the effectiveness of the proposed circuit. The paper is concluded in Section VI.

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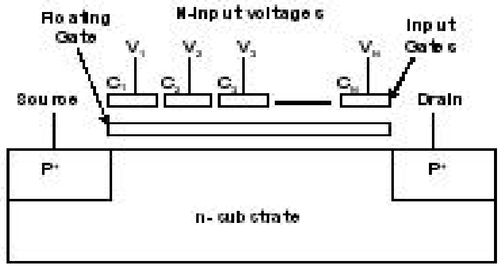

Fig. 1. Structure of an N-input FGMOS transistor

II. Operation of FGMOS

The structure of a typical N-input FGMOS is shown in Fig. 1. The voltage on the floating gate (V_{FG}) is expressed as [18]:

$$V_{FG} = \frac{\sum_{i=1}^{N} C_i V_i + C_{fd} V_{DS} + C_{fs} V_{SS} + C_{fb} V_{BS} + Q_{FG}}{C_T} \quad (1)$$

where C_1,C_2,C_3....,C_N are the input capacitances between control gate and floating gate, $\sum_{i=1}^{N} C_i$ is the sum of N-input capacitances, C_{fd} is the overlap capacitances between floating-gate and drain, C_{fs} is the overlap capacitances between floating-gate and source and C_{fb} is the parasitic capacitance between floating gate and substrate, V_i is the input voltage of i^{th} input gate , V_{DS} is the drain-to-source voltage, V_{SS} is the source voltage and V_{BS} is the substrate- to-source voltage, C_T is the total capacitance of the floating-gate and Q_{FG} is the residual charge.

The total capacitance is given as:

$$C_T = \sum_{i=1}^{N} C_i + C_{fd} + C_{fs} + C_{fb} \quad (2)$$

The residual charge at the floating gate can be neglected using method suggested in [19]. Therefore equation (1) reduces to:

$$V_{FG} = \frac{\sum_{i=1}^{N} C_i V_i + C_{fd} V_{DS} + C_{fs} V_{SS} + C_{fb} V_{BS}}{C_T} \quad (3)$$

If

$$\sum_{i=1}^{N} C_i >> C_{fd}, C_{fs}, C_{fb}, \quad (4)$$

then equations (2) and (3) are modified as:

$$C_T = \sum_{i=1}^{N} C_i \quad (5)$$

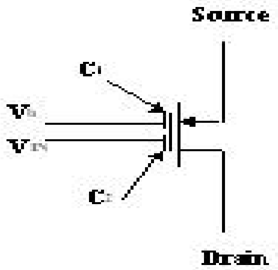

Fig. 2. Two-input FGMOS transistor

$$V_{FG} = \frac{\sum_{i=1}^{N} C_i V_i}{C_T} \tag{6}$$

The current equation for the N-input FGMOS has been obtained by modifying the conventional MOSFET equation. The current I_p in the saturation region is expressed as follows:

$$I_p = \frac{K_p}{2}\left\{V_{DD} - \left(\frac{\sum_{i=1}^{N} C_i V_i}{C_T}\right) + |V_{Tp}|\right\}^2 \tag{7}$$

where

$$K_p = \mu_p C_{OX} \frac{W}{L} \tag{8}$$

is the transconductance parameter, μ_p is the mobility, C_{OX} is the gate-oxide capacitance per unit area, W/L is the aspect ratio of the transistor, and V_{Tp} is the threshold voltage of the FGMOS. In the 2-input FGMOS transistor shown in Fig. 2, voltages V_b (dc bias voltage) and V_{IN} (input voltage) are applied at the two terminals. Due to the bias voltage V_b the threshold voltage V_{Tp} adjusts itself to a new value $V_{Tp,equ}$:

$$V_{Tp,equ} = \frac{V_{Tp} - V_b k_{11}}{k_{12}} \tag{9}$$

where $k_{11} = C_1/C_T$, $k_{12} = C_2/C_T$ are the capacitive coupling ratio and $C_T(= C_1 + C_2)$ is the total capacitance of the floating-gate. By choosing appropriate values of V_b, k_{11}, and k_{12} in (9), the threshold voltage $(V_{Tp,equ})$of the FGMOS becomes lower than the threshold voltage (V_{Tp}) of the conventional MOSFET [20].

III. FGMOS Based Squarer

The proposed FGMOS based squarer is shown in Fig. 3. The squaring function is being performed by M_1, M_2, M_3, and M_4 which are 2-input FGMOS transistors, whereas M_5, M_6, M_7, and M_8 which are used for proper biasing are MOS transistors. All these transistors are biased in the saturation region. The transistors M_1, M_2, M_3, and M_4 are perfectly matched i.e.

$$K_{pi} = K_p, V_{Tpi} = V_{Tp}, and k_{i1} = k_{i2} = k_1 \tag{10}$$

where i=1, 2, 3, 4. The transistors M_5 and M_6 form the current mirror and M_7 and M_8 set the bias current. From Fig. 3, it is evident that there is no body effect. The output current I_o is given as

$$I_o = I_1 - I_2 = (I_{p1} + I_{p2}) - (I_{p3} + I_{p4}) \tag{11}$$

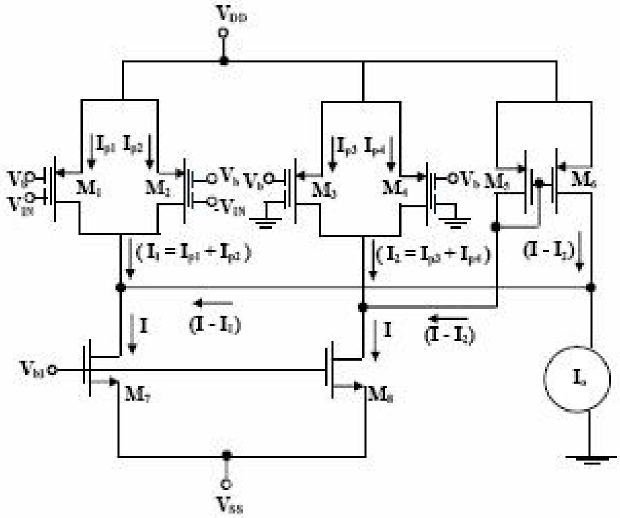

Fig. 3. Proposed FGMOS based squarer

where I_{p1}, I_{p2}, I_{p3}, and I_{p4} are the currents through M_1, M_2, M_3, and M_4 respectively and are obtained using (7), as follows

$$I_{p1} = \frac{K_p}{2}\left\{V_{DD} - k_1(V_b + V_{IN}) + |V_{Tp}|\right\}^2 \tag{12}$$

$$I_{p2} = \frac{K_p}{2}\left\{V_{DD} - k_1(V_b - V_{IN}) + |V_{Tp}|\right\}^2 \tag{13}$$

$$I_{p3} = \frac{K_p}{2}\left\{V_{DD} - k_1 V_b + |V_{Tp}|\right\}^2 \tag{14}$$

$$I_{p4} = \frac{K_p}{2}\left\{V_{DD} - k_1 V_b + |V_{Tp}|\right\}^2 \tag{15}$$

where V_{IN} is the input voltage, V_b is the bias voltage of FGMOS, and V_{DD} is the supply voltage. Substituting equations (12)- (15) in (11), we get:

$$I_o = K_p k_1^2 V_{IN}^2 \tag{16}$$

From equation (16), it is clear that the output current I_o is dependent upon input voltage and independent of the bias voltage V_b. The proposed squarer requires a fully differential input voltage with a proper common-mode DC voltage, which is provided by bias voltage V_b . If the capacitive coupling ratio is chosen as $K_1 = C_1/C_T = 0.5$ and the bias voltage V_b is connected to the power supply V_DD , the squarer will be biased at half of the supply voltage. From equation (5) it is clear that the input dynamic range of the squarer has increased. It is observed from the above analysis that the bias voltage V_b in 2-input FGMOS reduces the threshold voltage as well as increases the input dynamic range.

IV. Second Order Effects

In this section the effects of channel length modulation and mobility degradation on the proposed squarer are discussed.

1) Channel Length Modulation Effect: The current I_p of 2-input FGMOS including channel length modulation effect is

$$I_p = \frac{K_p}{2}\left\{V_{DD} - k_1(V_b + V_{IN}) + |V_{Tp}|\right\}^2 (1+\lambda V_{DS}) \quad (17)$$

where λ is the channel length modulation parameter. Considering this effect, equations (12)- (15) are modified as

$$I_{p1} = \frac{K_p}{2}\left\{V_{DD} - k_1(V_b + V_{IN}) + |V_{Tp}|\right\}^2 (1 + \lambda V_{DS1}) \quad (18)$$

$$I_{p2} = \frac{K_p}{2}\left\{V_{DD} - k_1(V_b - V_{IN}) + |V_{Tp}|\right\}^2 (1 + \lambda V_{DS2}) \quad (19)$$

$$I_{p3} = \frac{K_p}{2}\left\{V_{DD} - k_1 V_b + |V_{Tp}|\right\}^2 (1 + \lambda V_{DS3}) \quad (20)$$

$$I_{p4} = \frac{K_p}{2}\left\{V_{DD} - k_1 V_b + |V_{Tp}|\right\}^2 (1 + \lambda V_{DS4}) \quad (21)$$

Substituting equations (18)-(21), $V_{DS1} = V_{DS2}$ and $V_{DS3} = V_{DS4}$ in equation (11), we get:

$$\begin{aligned} I_o &= K_p k_1^2 V_{IN}^2 (1 + \lambda V_{DS1}) \\ &\quad + K_p \lambda (V_{DD} - k_1 V_b + |V_{Tp}|)^2 (V_{DS1} - V_{DS3}) \end{aligned} \quad (22)$$

For smaller values of drain-to source voltages V_{DS1} and $(V_{DS1} - V_{DS3})$, the effect of channel length modulation in (22) can be neglected.

2) Mobility Degradation Effect: The current I_p of 2-input FGMOS including mobility degradation effect is

$$I_p = \frac{K_p}{2}\frac{(V_{DD} - k_1(V_b + V_{IN}) + |V_{Tp}|)^2}{(1 + \theta(V_{DD} - k_1(V_b + V_{IN}) + |V_{Tp}|))} \quad (23)$$

In (23), $\theta(V_{DD} - k_1(V_b + V_{IN}) + |V_{Tp}|) << 1$, where θ is the mobility degradation parameter. Using Taylor's series expansion and neglecting the higher order terms, equation (23) is approximated as

$$\begin{aligned} I_p &= \frac{K_p}{2}(V_{DD} - k_1(V_b + V_{IN}) + |V_{Tp}|)^2 \\ &\quad * (1 - \theta(V_{DD} - k_1(V_b + V_{IN}) + |V_{Tp}|)) \end{aligned} \quad (24)$$

Considering this effect, equations (12)- (15) are modified as

$$\begin{aligned} I_{p1} &= \frac{K_p}{2}(V_{DD} - k_1(V_b + V_{IN}) + |V_{Tp}|)^2 \\ &\quad * (1 - \theta(V_{DD} - k_1(V_b + V_{IN}) + |V_{Tp}|)) \end{aligned} \quad (25)$$

$$\begin{aligned} I_{p2} &= \frac{K_p}{2}(V_{DD} - k_1(V_b - V_{IN}) + |V_{Tp}|)^2 \\ &\quad * (1 - \theta(V_{DD} - k_1(V_b - V_{IN}) + |V_{Tp}|)) \end{aligned} \quad (26)$$

$$\begin{aligned} I_{p3} &= \frac{K_p}{2}(V_{DD} - k_1 V_b + |V_{Tp}|)^2 \\ &\quad * (1 - \theta(V_{DD} - k_1 V_b + |V_{Tp}|)) \end{aligned} \quad (27)$$

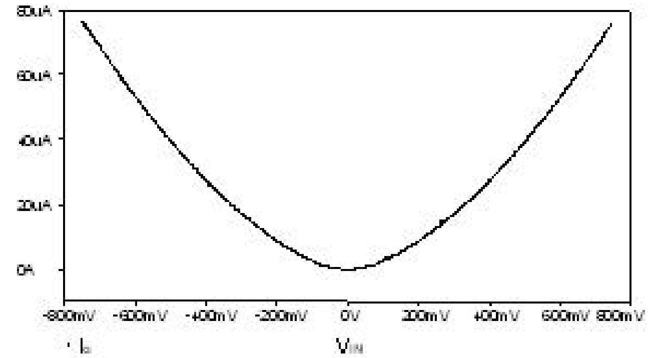

Fig. 4. I-V characteristic of the proposed squarer

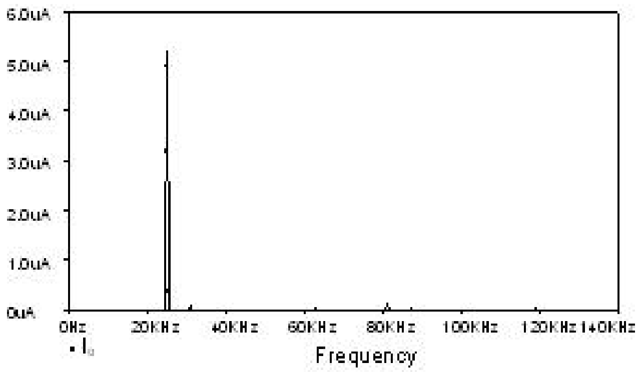

Fig. 5. Frequency spectrum of the proposed squarer for V_{IN} = $0.75V_{PP}$.

$$\begin{aligned} I_{p4} &= \frac{K_p}{2}(V_{DD} - k_1 V_b + |V_{Tp}|)^2 \\ &\quad * (1 - \theta(V_{DD} - k_1 V_b + |V_{Tp}|)) \end{aligned} \quad (28)$$

Substituting equations (25)-(28) in equation (11), we get

$$I_o = K_p k_1^2 V_{IN}^2 (1 - 3\theta(V_{DD} - k_1 V_b + |V_{Tp}|)) \quad (29)$$

From equation (29), we see that the term $(V_{DD} - k_1 V_b + |V_{Tp}|) << 1$, causes only the gain error. Since output current is the square of the input voltage, mobility degradation effect can be neglected.

V. Simulation Results

The proposed squarer circuit has been simulated using SPICE in $0.25\mu m$ CMOS technology. The squarer operates at the supply voltages of $\pm 0.75V$. Fig. 4 shows the simulation results of the squarer. The I-V characteristic in Fig. 4 shows the squaring function behaviour for the input voltages (V_{IN}) from $-0.75V$ to $0.75V$. The spectrum of the output waveform is shown in Fig. 5. From Fig. 5, it is observed that the total harmonic distortion (THD) is less than 1% for the input voltage V_{IN} = $0.75V_{PP}$. The simulation results are consistent with the theoretical results calculated by (16). The total power dissipation of the proposed circuit is 319μW.

VI. Conclusion

In this paper a new low-voltage FGMOS based squarer has been proposed. The proposed squarer operates at the supply voltages of $\pm 0.75V$. It has rail-to-rail input range, low power dissipation and fairly low THD. The analysis of the channel length modulation and mobility degradation effects show that they have little influence on the proposed squarer circuit. The simulation results have been presented to demonstrate the feasibility of the proposed squarer.

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