

Bode Stability Analysis for Single Wall Carbon Nanotube Interconnects Used in 3D-VLSI Circuits

Saeed H. Nasiri, Rahim Faez, Bitia Davoodi, and Maryam Farrokhi

Abstract—Bode stability analysis based on transmission line modeling (TLM) for single wall carbon nanotube (SWCNT) interconnects used in 3D-VLSI circuits is investigated for the first time. In this analysis, the dependence of the degree of relative stability for SWCNT interconnects on the geometry of each tube has been acquired. It is shown that, increasing the length and diameter of each tube, SWCNT interconnects become more stable.

Keywords—Bode stability criterion, Interconnects, Interlayer via, Single wall carbon nanotubes, Transmission line method, Time domain analysis

I. BACKGROUND

AS process technology continues to scale downward, traditional copper interconnects in high-performance very large scale integration (VLSI) systems will suffer from serious problems such as restricted max current density, low electrical and thermal conductivity and short mean free path [1], [2]. Over the last decade we have witnessed tremendous advances in the characterization of structure and electrical properties of carbon nanotubes (CNTs) [3]. Because of high mechanical and thermal stability, high thermal conductivity and large current carrying capacity, CNTs have aroused a lot of research interest in their applicability as VLSI interconnects of the future. Bundles of metallic single-walled CNTs (SWCNTs) with electron mean free paths of the order of a micron are the most suitable candidates for interconnects [4]. In addition, this innovative material shows significant properties in terms of thermal dissipation and reliability, so it is proposed to realize both horizontal and vertical interconnections at chip and package level for future VLSI ultrascaled technologies. The fabrication technology for these bundles is well-assessed for vertical vias where high density bundles with low contact resistance have been realized [5].

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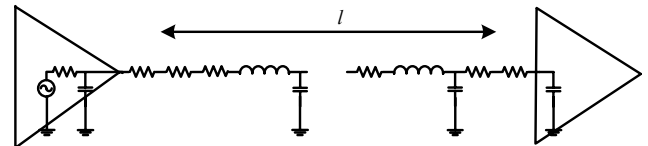


Fig. 1 RLC schematic of transmission line circuit model for a driver-SWCNT interconnect-load configuration

Fig. 1 illustrates a schematic representation of a typical RLC model for a SWCNT bundle interconnect made of N SWCNTs of the same lengths l and diameters D . In this figure, R_C , R_Q , and R_S represent the equivalent resistances introduced by the imperfect contacts, the quantum effect, and the carriers' scatterings, respectively. One can approximate the quantum contact resistance as $R_Q \approx h \{2e^2 N_{ch} N\}^{-1}$ [6], wherein h , e , and N_{ch} are the Plank's constant, electron charge, and number of conducting channels in each SWCNT. When the length of each SWCNT is greater than its carriers' mean free path (λ), the equivalent distributed ohmic resistance (per unit length) introduced by carriers scatterings with defects, substrate-induced disorders, and phonons can be written as $R_S \equiv R_Q / \lambda$ [6]. Also shown in Fig. 1; $C_E \approx 2\pi\epsilon / (N \ln(y/D))$ [7] in which ϵ is the dielectric permittivity, y is distance of SWCNT bundle from ground plane, and D is diameter of each tube. $C_Q \approx \{R_Q v_F\}^{-1}$ is the per unit length values of the equivalent capacitances induced by the electrostatic and quantum effects, respectively, in which v_F is the Fermi velocity in graphite.

Since the separation between any two SWCNT is much smaller than y , the effect of the electrostatic capacitances between any two SWCNT in the bundle is negligible. Furthermore, $L_K = R_Q / v_F$ and $L_M \approx \mu \times \ln(y/D) / (2\pi N)$ [7] represent the per unit length values of the kinetic and the magnetic inductances, in presence of the ground plane, wherein μ is the CNT permeability. In a practical case $L_M \ll L_K$ [6].

In order to obtain the number of conducting channels in each SWCNT, one can add up contributions from all electrons in all n_C conduction sub-bands and all holes in all n_V valence sub-bands [8]:

$$N_{ch} = \sum_{i=1}^{n_C} \left[e^{(E_i - E_F)/kT} + 1 \right]^{-1} + \sum_{i=1}^{n_V} \left[e^{(E_i + E_F)/kT} + 1 \right]^{-1} \quad (1)$$

where $i(=1, 2, 3, \dots)$ is a positive integer, E_F , k , and T are the

Fermi energy, the Boltzmann constant, and temperature, respectively, and E_i represents the quantized energy that corresponds to the i -th conduction or valence subband. This quantization is due to diameter confinement, introduced by the tube's finite diameter.

The system studied in this research is shown in Fig2. Two horizontal tracts have been considered on two layers, connected together by a via, where both top and bottom layers as well as via are CNT bundles.

Despite valuable properties there are several prospects to be investigated for practical use of carbon nanotube interconnects. Following this stream, here, the stability analysis of on-chip CNT interconnects has been studied, considering both horizontal traces and vertical vias. In this paper, Bode analysis has been used as a criterion to study relative stability by changing the geometry of CNTs, and MATLAB software for approaching the stability issue.

In Bode' plots, magnitude (in db) and phase are plotted against frequency and we can see large ranges of gain because the db scale presents information differently. The gain margin (GM) and phase margin (PM) provide measures of how close a system is to a stability limit. Phase margin is just the difference between -180° and the actual phase angle of the frequency response function, measured at the frequency where the magnitude of the frequency response function, is equal to one (0 db). Gain margin is just the amount of gain that we can add to move the zero db crossing to occur at the same frequency as the -180° crossing. The system becomes more stable if the GM and PM increase [9].

II. MATRIX FORMULATION

In Fig. 1, a SWCNT bundle interconnect is shown with the length l that is represented by a series of distributed resistances (R_S), inductances (L), and capacitances (C) (all in per length units) Such interconnect is applied to both horizontal and vertical structures and these are driven by a driver with an output resistance R_{out} and an output capacitance C_{out} . The SWCNT bundle interconnects is also connected to a load of capacitance C_L .

In order to calculate the input-output transfer function of the configuration in Fig. 1, total transmission parameter matrix should be derived. For this purpose ABCD transmission parameter matrix are used for a uniform RLC transmission line of length l that contains N_B distributed blocks. Accordingly, total ABCD transmission parameter matrix is defined as:

$$T_{total} = \begin{bmatrix} A_T & B_T \\ C_T & D_T \end{bmatrix} \equiv \begin{bmatrix} 1 & R_{out} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ sC_{out} & 1 \end{bmatrix} \begin{bmatrix} 1 & R_{ex} \\ 0 & 1 \end{bmatrix} \times \begin{bmatrix} 1 + (R_S dx + Ldxs) sCdx & (R_S dx + Ldxs) \\ sCdx & 1 \end{bmatrix}^{N_B} \begin{bmatrix} 1 & R_{ex} \\ 0 & 1 \end{bmatrix} \quad (2)$$

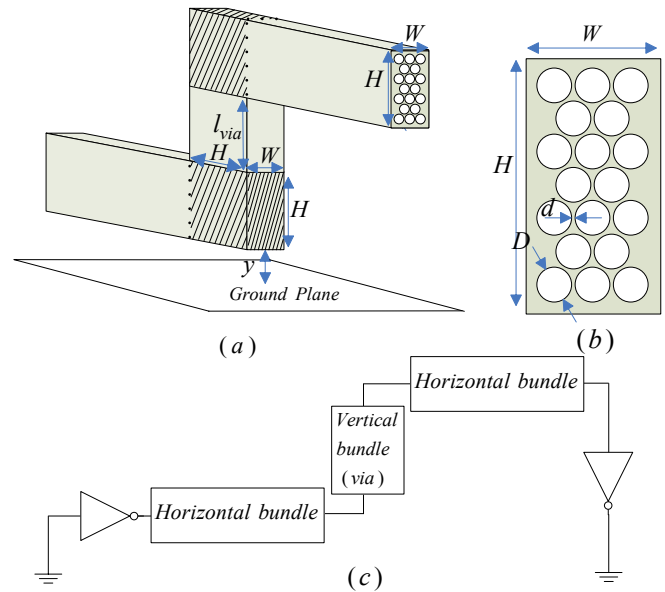


Fig. 2 Schematic of a) 3D VLSI structure; b) cross-section of the bundles; c) complete schematic

Where $R_{ex}=(R_C+R_Q)/2$, $L=L_K+L_M$, $C=C_E C_Q/(C_E+C_Q)$, $dx=l/N_B$, and $s=j\omega$ is the complex frequency. We obtain the linear parametric equivalent for the transfer function of as:

$$H(s) = \frac{V_o(s)}{V_i(s)} = \frac{1}{A_T + sC_L B_T} \quad (3)$$

Since a combination of the two horizontal and a vertical structures is used here, the formula in (3), will be devised as:

$$H(s) = \frac{V_{o1}(s)}{V_i(s)} \times \frac{V_{o2}(s)}{V_{o1}(s)} \times \frac{V_o(s)}{V_{o2}(s)} \quad (4)$$

III. BODE STABILITY ANALYSIS

By varying the nanotubes' dimensions, ($2 \mu m \leq l \leq 6 \mu m$ and $3 \text{ nm} \leq D \leq 7 \text{ nm}$) and generating various Bode diagrams, we have studied the effect of SWCNT bundle geometry on the relative stability of the configuration given in Fig. 2(c). All geometrical and physical parameters are according to the 22-nm technology node, extracted from ITRS2009 [2]. Both horizontal local interconnects are assumed to have ideal contact (i.e., $R_C=0$) [2]. The driver size is set to be 100 times the minimum sized gate for the 22-nm technology node, given in [2]. The bundle width is 22 nm and its thickness is 44 nm. The values of N are 83, 32 and 15 for $D=3, 5$ and 7 respectively. The space between two adjacent CNTs is assumed as 0.34 nm and E_F as 0.3 eV. All individual SWCNTs are assumed to be metallic. In this analysis, we have

assumed the parameters in via as $l=80 \text{ nm}$, $R_C=21.22 \Omega$, $C_L=0$,

$C_{out}=0$, in top tract as $C_L=0$, $C_{out}=0.049e-15 \text{ fF}$, and in bottom

tract as $C_L=0.14e-15$ fF, $C_{out}=0$.

Bode diagrams are shown in Fig. 3 for the configuration of Fig. 2(c) regarding $l=2, 4, \text{ and } 6 \mu\text{m}$. The diameter of each tube is assumed to be 3 nm. As shown in Fig. 3, by increasing

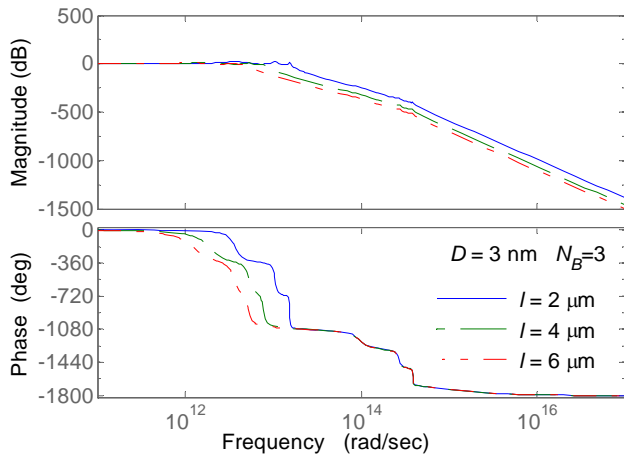


Fig. 3 The Bode diagrams for driver-SWCNT bundle interconnect-load configuration of Fig. 2(c) for $D=3$ nm and $2 \mu\text{m} \leq l \leq 6 \mu\text{m}$

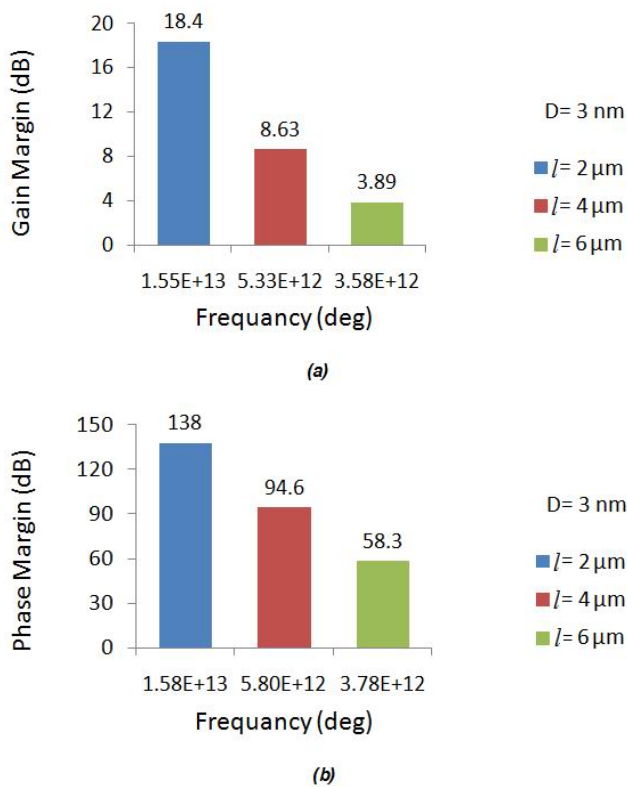


Fig. 4. (a) Decreasing the absolute values of gain margins versus frequency with $D=3$ nm and $2 \mu\text{m} \leq l \leq 6 \mu\text{m}$; (b) Decreasing the absolute values of phase margins versus frequency

the length of CNTs, the gain margin and phase margin of interconnect increase; the details are depicted in Figs. 4(a) and 4(b). Thus, by increasing the length of CNT bundle, the system becomes more stable. This is because by increasing the length of tubes, the equivalence impedance of the interconnect increases so that the step response of the system go to more

damping and the system tend to be more stable.

Bode diagrams for $D=3, 5, \text{ and } 7$ nm is illustrated in Fig. 5. The length of each tube is assumed to be $2 \mu\text{m}$. As shown in

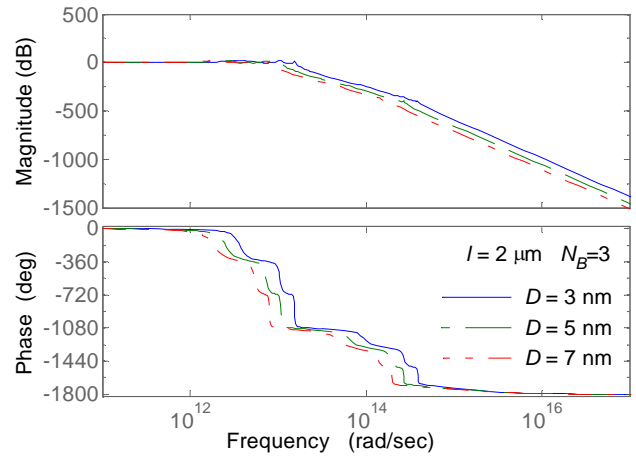


Fig. 5 The Bode diagrams for driver-SWCNT bundle interconnect-load configuration of Fig. 2(c) for $l=2 \mu\text{m}$ and $3 \text{ nm} \leq D \leq 7 \text{ nm}$

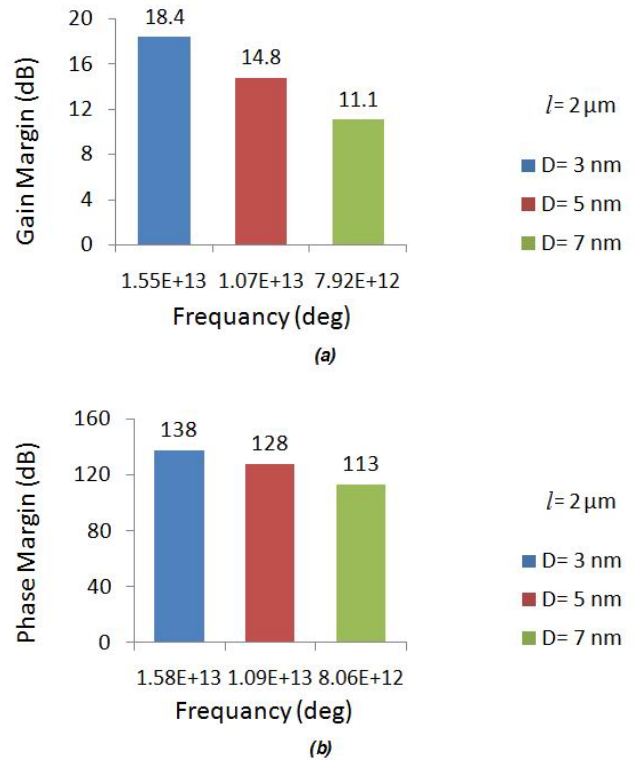


Fig. 6 (a) Decreasing the absolute values of gain margins versus frequency with $l=2 \mu\text{m}$ and $3 \text{ nm} \leq D \leq 7 \text{ nm}$; (b) Decreasing the absolute values of phase margins versus frequency

Fig. 5, gain margin and phase margin of interconnect increase as the diameter of each tube increases; therefore, the system becomes more stable. This is because by increasing the tube diameters the bundle becomes less dense and its conductivity decreases so that its step response tends to be more damping. The relevant details are depicted in Figs. 6(a) and 6(b).

The present general analysis whose transfer function is of the order of 20, provides much more accurate and realistic numerical results than those that could be obtained by similar analyses presented in [10] with order of four and [11] with the order of six both for SWCNT-bundle interconnects, and in [12] with the order of four for multi layer graphene nanoribbon (MLG NR) interconnects.

IV. CONCLUSION

In the analysis presented in this paper relative stability analysis for single wall carbon nanotube interconnects used in 3D-VLSI circuits is investigated. Using transmission line modeling along with Bode stability diagrams, we have shown that with increasing the length or diameter of each tube, the relative stability increases and hence the system will be more stable. This is because any increase in the parameters will cause switching delay; therefore, the system's step response tends to damp faster and consequently the system will be more stable.

REFERENCES

- [1] A. Nieuwoudt, and Y. Massoud, "Understanding the Impact of Inductance in Carbon Nanotube Bundles for VLSI Interconnect Using Scalable Modeling Techniques," *IEEE Transactions on Nanotechnology*, vol. 5, pp 758-765, Nov. 2006.
- [2] International Technology Roadmap for Semiconductors (ITRS), 2009. <http://www.itrs.net>
- [3] B. Q. Wei, R. Vajtai, and P. M. Ajayan, "Reliability and current carrying capacity of carbon nanotubes," *Applied physics letters*, vol. 79, pp 1172-1174, July 2001.
- [4] Kaustav Banerjee, Sungjun Im, and Navin Srivastava, "Interconnect Modeling and Analysis in the Nanometer Era: Cu and Beyond," *Proceedings of the 22nd Advanced Metallization Conference*, Colorado Springs, Sep. 2005.
- [5] A.G. Chiariello, A. Maffucci, and G. Miano, "Signal Integrity Analysis of Carbon Nanotube on-chip Interconnects," *IEEE Signal Propagation on Interconnects*, Strasbourg, pp. 1-4, June 2009.
- [6] N. Srivastava and K. Banerjee, "Performance analysis of carbon nanotube interconnects for VLSI applications," in *IEEE ICCAD*, pp. 383-390, Nov. 2005.
- [7] W. H. Hayt, and J. A. Buck, "Engineering Electromagnetics," 7th Ed. New York: McGraw-Hill, 2005.
- [8] A. Naeemi and J. D. Meindl, "Compact physical models for multiwall carbon-nanotube interconnects," *IEEE Electron Device Lett.*, vol. 27, no. 5, pp. 338-340, May 2006.
- [9] R. C. Dorf, R. H. Bishop, *Modern Control System*, 11th Ed., Englewood Cliffs, NJ: Prentice-Halls, 2008.
- [10] D. Fathi, and B. Forouzandeh, "A Novel Approach for Stability Analysis in Carbon Nanotube Interconnects," *IEEE Electron Device Lett.*, vol. 30, pp. 475-477, Apr. 2009.
- [11] D. Fathi, B. Forouzandeh, S. Mohajerzadeh, and R. Sarvari, "Accurate analysis of carbon nanotube interconnects using transmission line model," *Micro & Nano letters*, vol. 4, pp. 116-121, Jul. 2009.
- [12] S. H. Nasiri, M. K. Moravvej-Farshi, and R. Faez, "Stability Analysis in Graphene Nanoribbon Interconnects," *IEEE Electron Device Lett.*, vol. 31, pp. 1458-1460, Oct. 2010.

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