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Analysis of CNT Bundle and its Comparison with Copper for FPGAs Interconnects

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Abstract**—**Each new semiconductor technology node brings smaller transistors and wires. Although this makes transistors faster, wires get slower. In nano-scale regime, the standard copper (Cu) interconnect will become a major hurdle for FPGA interconnect due to their high resistivity and electromigration. This paper presents the comprehensive evaluation of mixed CNT bundle interconnects and investigates their prospects as energy efficient and high speed interconnect for future FPGA routing architecture. All HSPICE simulations are carried out at operating frequency of 1GHz and it is found that mixed CNT bundle implemented in FPGAs as interconnect can potentially provide a substantial delay and energy reduction over traditional interconnects at 32nm process technology.

Keywords**—**CMOS**,** Copper Interconnect, Mixed CNT Bundle Interconnect, FPGAs.

I. INTRODUCTION

FPGAs (field programmable gate arrays) offer an attractive solution for significantly lowering the amortized manufacturing cost per unit and dramatically improving design productivity through reuse of the same silicon implementation for a wide range of applications. More importantly, FPGA is programmable and can be reconfigured for yield improvement and defect tolerance. These features become absolutely necessary when CMOS technology scales down to nanometer scale [1]. The major performance and power bottleneck of the FPGA is the programmable interconnects and routing elements inside the FPGA. These have been found to account up to 80% of the total delay and up to 85% of the total power consumption [2]. One promising way to improve FPGA interconnect performance is to incorporate mixed carbon nanotubes bundle interconnects instead of traditional copper interconnect.

Carbon nanotubes (CNTs) have been proposed as possible replacements for copper interconnect due to their large conductivity and current carrying capabilities [3]-[7]. CNTs can be thought of being made by rolling up a single atomic layer of graphite to form a seamless cylinder. The resulting structure is called single-walled carbon nanotube (SWCNT) [8] as shown in Fig. 1(a). If several SWCNTs with varying diameter are nested concentrically inside one another, then the resulting structure is called as multi-walled carbon nanotube (MWCNT) [9], as shown in Fig.1 (b). The SWCNT consists of one grapheme shell, whereas the MWCNT has multishells [10]. However, the individual SWCNTs suffer from a high ballistic resistance of 6.5kΩ. To reduce the impact of individual tube, bundles of SWCNTs in parallel are required to provide high conductance. Almost all experimental results have demonstrated that a realistic nanotube bundle contains a mixed bundle of SWCNTs and MWCNTs. Depending on the process controls and conditions during CNT synthesis, the diameters of the CNTs inside a bundle follow normal distributions [11]-[13].

This paper analyses the various design aspects of mixed CNT bundle and investigates the prospects of mixed bundle of CNTs as future FPGAs interconnects. All simulations are carried out at 32nm technology node at operating frequency of 1GHz. The paper is organized as follows. Section II describes the conductance of CNT bundle**.** Section III describes the inductance and capacitance of CNT bundle. Section IV compares the conductance of CNT and Cu interconnects. Section V explains the architecture of target FPGAs. Section VI compares the performance of FPGAs with mixed bundle and traditional interconnects and section VII concludes this paper.

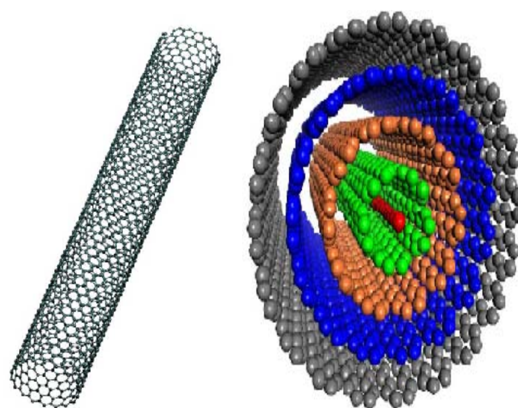

Fig.1 (a) Single-walled CNT (b) Multi-walled CNT

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II. Conductance of CNT Bundle

The conduction of an SWCNT or MWCNT is determined by two parameters: the conducting channel per shell and the number of shells. A SWCNT has one shell, whereas the number of shells (N_{sh}) in MWCNT depends on diameter [10].

$$Nsh = 1 + \frac{(Dout - Din)}{2\delta} \quad (1)$$

Where D_{out} and D_{in} are the maximum and minimum shell diameter and δ is the van der Waals distance between graphene layers in graphite (which is 0.34nm). Fig. 2 shows the simulation results of different process parameters such as tube density (D), the ratio D_{in} / D_{out} (R) and probability of metallic CNTs (r) in a bundle. For the same aspect ratio of a CNT bundle if the D varies from 1E+12 to 5E+12 tubes / cm^2 the numbers of tubes in the bundle increases from 21 to 90. Similarly the variation of r from 1/3 to 2/3 increases the number of conduction channels from 256 to 312. The variation of R ratio impacts the number of the shells of MWCNTs. A smaller R ratio leads to more shells and a higher conductance. Simulation results shows that compared to (D= 1E+12, r=0.33 and R=0.5) the process parameters (D= 5E+12, r=0.667 and R=0.3) improves the bundle conductance by 10X. Hence the proper selection of above parameters decides the improvement in bundle conduction.

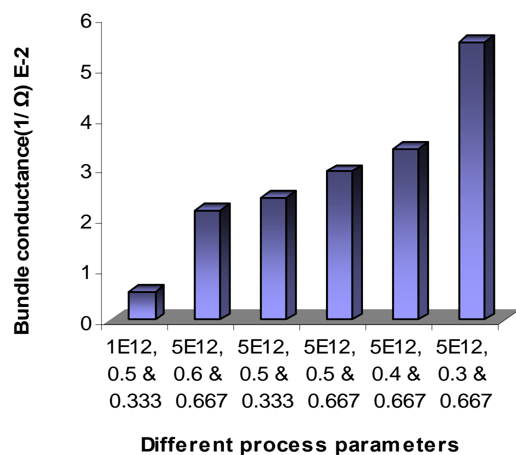

Fig. 2 Bundle conductance Vs process parameters (D, R & r)

III. Inductance And Capacitance Of CNT Bundle

A) Inductance: The CNT has two types of inductances, magnetic inductance and kinetic inductance. The magnetic inductance depends on the magnetic field inside and between the tubes. Whereas kinetic inductance is the kinetic energy of electrons, which is per unit length for each conduction channel in a CNT shell. To analyze the contribution of both inductance types a simulation has carried out for a bundle geometry of [width (W) = height (H) for interconnect length (L) =10um) with other process parameter constant, it is found that as W increases the magnetic inductance starts to fall, whereas due to constant number of conduction channel (as R fixed) the kinetic inductance remains constant. Hence the total inductance (kinetic + magnetic) falls gradually with W as shown in Fig.3. Hence for a significant reduction into total inductance, it's required to see the reduced contribution of magnetic inductance also.

The kinetic inductance (L_K) per conduction channel is given by [14]

$$LK = \frac{hL}{4e^2 vfNc} \quad (2)$$

Where *h* is planks constant, *e* is the charge of single electron, vf is the Fermi velocity in graphite, Nc is the number of conduction channels and *L* is the length of CNTs. This shows that the kinetic inductance of a bundle is inversely proportional to number of conduction channels. As per discussion in Section I by lowering the R we can create more conduction channels, and hence can lower the kinetic inductance. Simulation results of Fig.4 for bundle geometry of (W=H=50nm and L=10um) shows, that compared to (D= 5E+12, r=0.33 and R=0.6) the process parameters (D= 5E+12, r=0.667 and R=0.3) reduces the kinetic inductance by 67%.

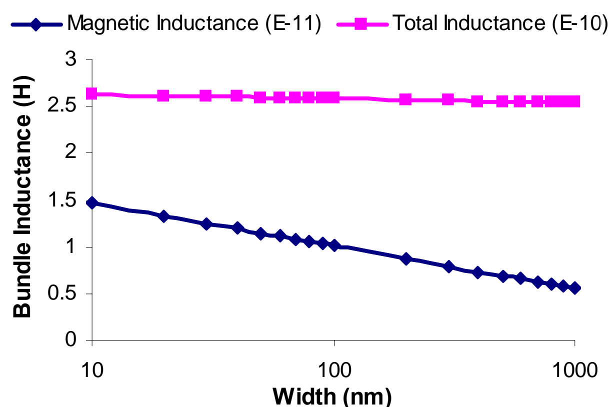

Fig. 3 Inductance Vs bundle width (W)

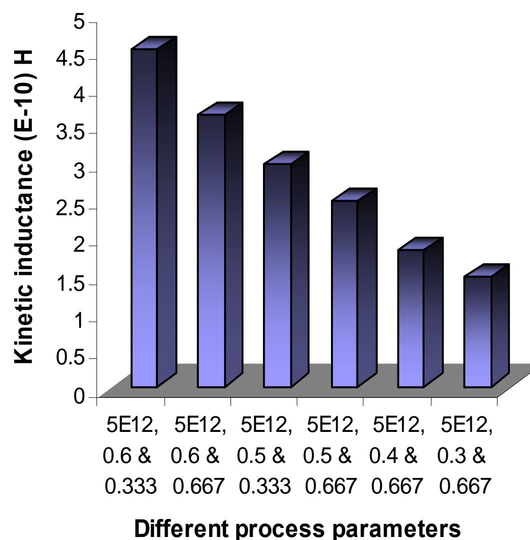

Fig. 4 Kinetic inductance Vs process parameters (D, R & r)

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Similarly Fig.5 shows the simulation results of the above geometry bundle with respective to average diameter of tubes. As the average diameter increases from 2.5 to 4nm the bundle has around 120 tubes and the number of conduction channels (*Nc*) increases from 271 to 421. This decreases the kinetic inductance from 2.96E-10 to 1.91E-10 Henry (which 35% less) respectively. Now as the average diameter reaches to 4.5nm, the numbers of tubes accompanied by the said bundle reduces from 120 to 105 therefore *Nc* falls from 421 to 312. This results in the increase of kinetic inductance from 1.91E-10 to 2.57 E-10 Henry. Beyond the average diameter of 4.5nm the density of tubes cross the limit of 5E+12 tubes / cm^2 therefore the simulations are restricted up to an average diameter of 4.5nm only. Hence it is important to choose the average diameter carefully so as to reduce the kinetic inductance of a given mixed CNT bundle for the selected tube density.

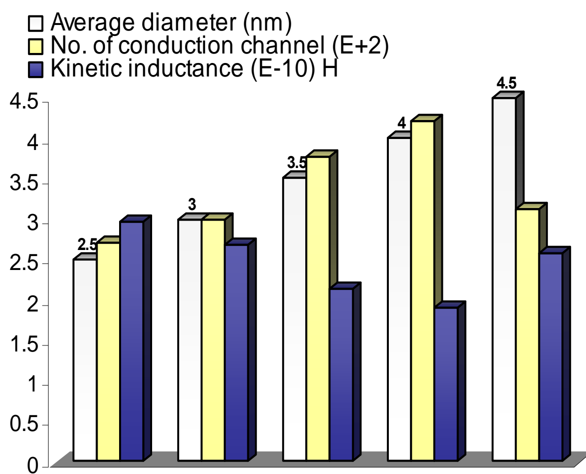

Fig. 5 Kinetic inductance Vs Average diameters

B) Capacitance: The capacitance of a CNT arises from two sources. The electrostatic capacitance (*Ce*) is calculated by treating the CNT a thin wire, with diameter 'd' which is placed a distance 'y' away from the ground plane and given by

$$Ce = \frac{2\Pi\varepsilon}{\ln(y/d)} \tag{3}$$

Whereas, the quantum capacitance (*Cq*) arises from the quantum electrostatic energy stored in the nanotube, when it carries the current. The *Cq* of each shell is given by [14]

$$Cq = \frac{4e^2 NcL}{hvf} \tag{4}$$

This shows that *Cq* is directly proportional to *Nc* subjected to *L* constant. When CNT carries the current then these two capacitance appears in series. Fig.6 shows the simulation results of (W=H =50nm and L= 10um) bundle geometry, as the average diameter increases from 2.5 to 4nm. The number of the tubes remains 120 and due to increasing number of subbands, *Nc* increases from 236 to 372, therefore *Cq* increases by 37%. As the average diameter approaches to 4.5nm, then the said bundle geometry accommodate only 105 tubes and Nc reduces to 256 from 372 which decreases the *Cq* by 31%. Hence the proper selection of average diameter is important because it decides the magnitude of *Cq*.

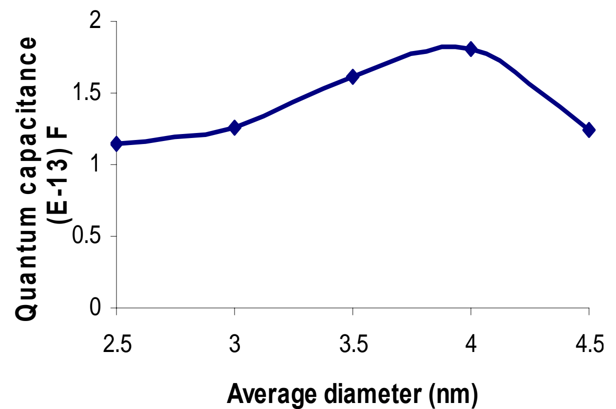

Fig. 6 Quantum capacitance (*Cq*) of bundle

IV. Conductance Of CNT And Cu Interconnects

As the process technology scales down in order to provide sufficient current and to minimize the electromigration, the conductor height-to-width aspect ratio of traditional copper interconnect continues to increase [15]. Since the CNTs can reliably handle three orders of magnitude larger current densities than copper conductor [16], CNTs-based interconnects potentially provide larger benefits in area. A mixed bundle of CNTs and Cu interconnects are modeled as equivalent transmission line and the equivalent circuit parameters (R, L, C) were extracted, using the Carbon Nanotubes Interconnect Analyzer (CNIA) [17] and BPTM tools [18], with the interconnects geometry suggested in [19]-[20]. Fig. 7 shows the comparison of conductance between the mixed CNT bundle and Cu for the same geometry. At lower bundle width (< 20nm) the number of tubes accompanied by the bundle are less and hence the conductance dropped, but still it is 5.7X the conductance of Cu.

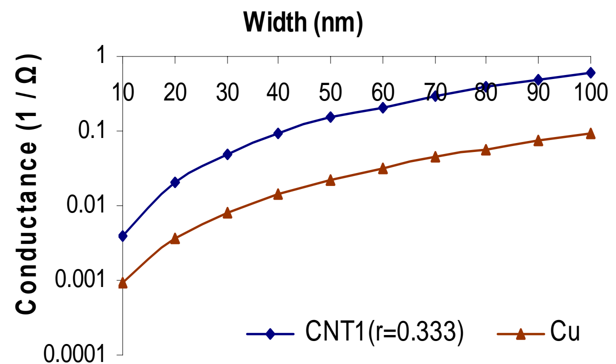

Fig.7 Conductance comparison of CNT bundle vs. Cu

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V. Architecture Of Target FPGA

This paper considered island-style FPGA architecture utilized by Xilinx [21] as shown in Fig. 8. The FPGA consists of a group of configurable logic blocks (CLBs) and programmable interconnect resources. A slice consists of 2 LUTs (Lookup-table) and 2 flip-flops. The CLBs access the interconnect fabric through connection blocks (CBs), and the inter-CLB wires are interconnected through switch blocks (SBs), which consists of variable length wire segment that connect to one another through programmable buffered switches, such as Double block, which drive a wire segment that span 2 CLB tiles, Hex blocks drive wires that span 6 CLB tiles and Long resources span the entire width or height of the FPGA as shown in Table 1. These resources typically consume approximately 70% of FPGA area and constitute the major portion of critical path delay and power consumption of most of FPGA design [22]. As the technology scales, the mixed CNT bundle have potentially less resistance than copper wires hence CNT may be a good choice for FPGA interconnect.

To measure the performance of the proposed interconnects, the conditions of a used switch in an actual FPGA were simulated using the test platform shown in Fig. 9. The test platform corresponds to a contiguous path of three switches through an FPGA routing fabric; the multiplexers in all three switches are configured to pass input 'In' to their outputs. Power and delay measurements are made for the second switch, labeled as "test switch".

TABLE I
Major Interconnects Present In The Switch Box

Interconnect Resources	Details
DOUBLE	16-to-1 multiplexer and buffer
XEH	12-to-1 multiplexer and buffer
LONGH	32-to-1 multiplexer and buffer

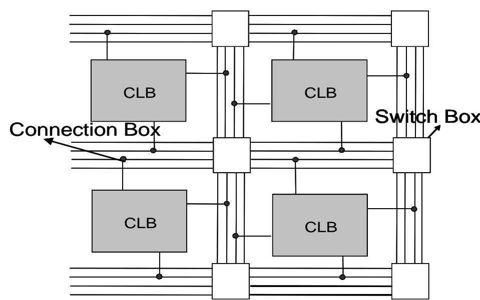

Fig. 8 Island-style FPGA architecture

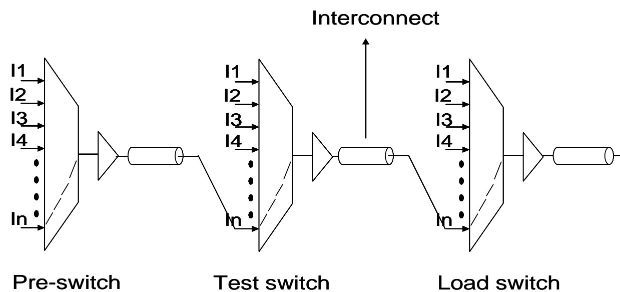

Fig. 9 Baseline test platform.

VI. Performance Comparison of CNT and Cu Interconnect For Target FPGAs

The equivalent RLC model of [6]is used for measuring the delay and power of CNT and Cu interconnects. The parameters (R, L, C) of interconnect were extracted, using the Carbon Nanotubes Interconnect Analyzer (CNIA) [17] and BPTM tools [18], with interconnect geometry suggested in [19, 20]. The segment length (between two CLB tile) for 32nm technology node considered is 17.7um [23]. All multiplexer in the SBs are made with minimum sized transistors with gate boosting of (VDD + Vth), which reduces the power consumption in level restoring buffer. The length of interconnect used for simulation for Double (2x 17.7um), Hex (6x 17.7um) and Long (24x 17.7) is 35.4um, 106.2um and 424.8um respectively. The Double, Hex and Long interconnect is implemented as intermediate and global interconnect respectively. Compared to Cu the CNT bundle interconnect has lower values of extracted R and C component, therefore the delay, power, energy and energy-delay-product

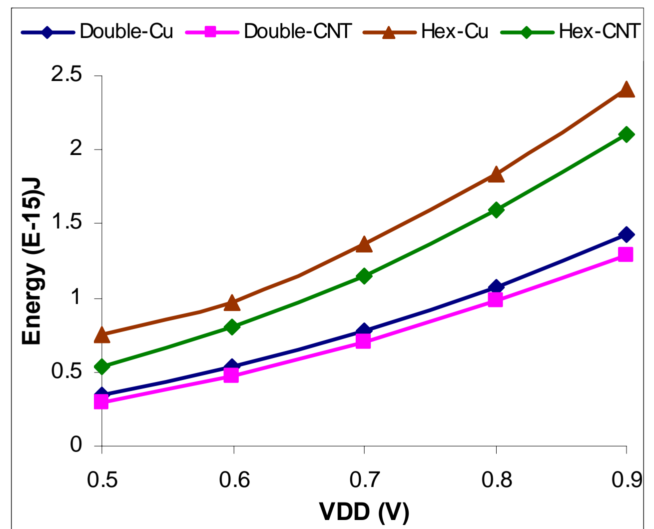

Fig. 10 Energy vs. VDD for Hex and Double interconnect

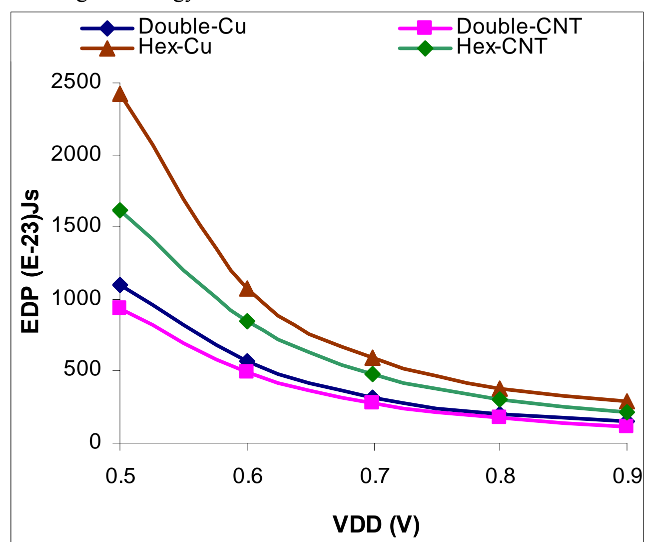

Fig. 11 EDP vs. VDD for Hex and Double interconnect

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(EDP) of Double, Hex and Long CNT interconnect is lower than that of implemented by Cu. At VDD = 0.9V, the Double and Hex CNT interconnect is 10.5% and 13% more energy efficient than Cu interconnect, similarly the EDP of CNT Double and Hex is 23% and 24.5% less than the EDP of Cu as shown in Fig. 10 and 11 respectively. Due to larger length of Long interconnect the advantage of delay, energy and EDP in case of CNT interconnect is more than Cu interconnect. Simulation results at VDD = 0.9V depicted in Fig. 12 shows that the Long CNT interconnect is 18% more energy efficient than Cu. Similarly the EDP of CNT Long is 30% less than the EDP of Cu as shown in Fig. 13.

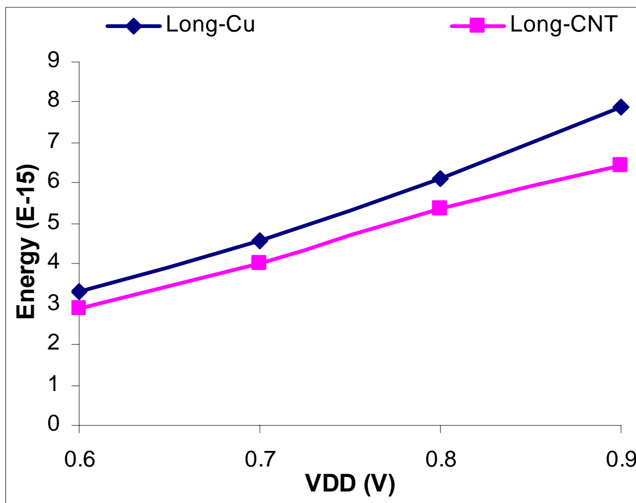

Fig. 12 Energy vs. VDD for Long interconnect

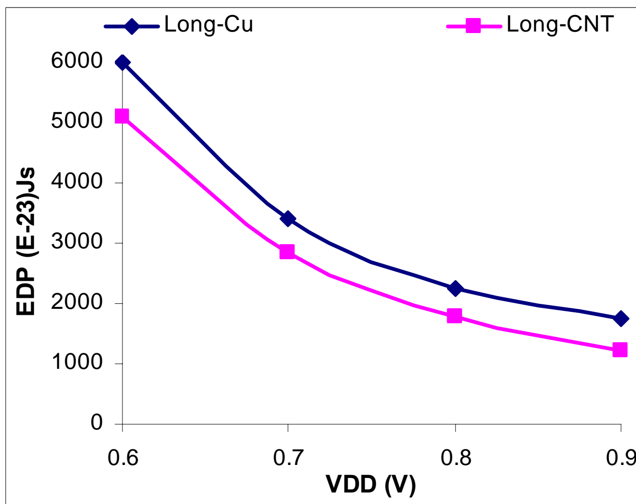

Fig. 13 EDP vs. VDD for Long interconnect

VII. Conclusion

This paper presents an analysis of mixed CNT bundle interconnect and compare it with Copper interconnect for future FPGA routing architecture. The results demonstrate that FPGAs that utilize mixed CNT bundle interconnect can provides an average 12% improvement in energy saving for Double and Hex line, further the longer interconnect such as Long lines provides 30% improvement in EDP. Our analysis results also point out that the tube density, tube distribution, metallic tube ratio, the ratio of *D*in/*D*out and bundle dimension are crucial factors in determining the inductance, capacitance and conductance performance of the mixed CNT bundle. The discussion on the selection of these CNT parameters can provide an important guideline for the design of mixed CNT bundles for future FPGAs interconnects.

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