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Complementary Energy Path Adiabatic Logic based Full Adder Circuit

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***Abstract*—**In this paper, we present the design and experimental evaluation of complementary energy path adiabatic logic (CEPAL) based 1 bit full adder circuit. A simulative investigation on the proposed full adder has been done using VIRTUOSO SPECTRE simulator of cadence in 0.18µm UMC technology and its performance has been compared with the conventional CMOS full adder circuit. The CEPAL based full adder circuit exhibits the energy saving of 70% to the conventional CMOS full adder circuit, at 100 MHz frequency and 1.8V operating voltage.

***Keywords*—**Adiabatic, CEPAL, full adder, power clock

I. Introduction

Adiabatic logic presents a promising alternative to conventional CMOS for the realization of low power electronics. Energy recovery techniques and adiabatic logic topologies minimizes energy dissipation by maintaining low voltage drop across conducting devices at all times. The un-dissipated energies related to the charges stored in the circuit capacitors are recycled. Thus the energy is not dissipated as heat. This method can usually be applied in addition to other approaches like power supply voltage reduction and algorithmic techniques for reduced logic transitions. In conventional CMOS logic we use constant voltage source to charge the load capacitance [13-16] whereas all adiabatic logic families are based on the time varying ramp voltage supply. The following mathematical analysis, based on time period (T), stored charge ($C_L V$), load capacitance C_L and channel resistance R is sufficient to understand adiabatic logic principle.

$$P_{diss} = 2(\frac{RC_L}{T})C_L V_{DD}{}^2 + V_t{}^2 C_L$$

Hence as given by above equation, keeping the clock transient time T much larger than intrinsic time constant RC_L of a device; we can reduce power dissipation in a switching transition. The extra power dissipation due to the threshold voltage drop (V_t) is classified as a non adiabatic loss [6].

Various adiabatic circuit topologies have been proposed over the past decade [1]-[12]. Most of these circuits have relied on multiple-phase power-clocks to steer currents and recycle charges [3]-[7]. They are not attractive for high speed design, due to their relative complex control requirements. In contrast to multiphase circuits, single phase adiabatic circuits [1, 2, 8] have simple clocking requirements, thus they enjoy minimal control overheads and are capable of operating at high speeds, while achieving high-energy efficiency. Complementary energy path adiabatic logic (CEPAL) inherits all the advantages of single phase adiabatic circuits [17] with additional improvement in robustness and throughput.

This paper describes the design and experimental evaluation of a 1 bit CEPAL full adder circuit. In addition to power/energy measurements, our paper includes a simulation based comparison of the proposed full adder with static CMOS full adder. A conventional CMOS adder with the same features i.e. no. of transistors, supply voltage, and frequency was also simulated and its performance was measured. CEPAL full adder was found to be more energy efficient than the CMOS full adder.

This paper has been segmented into six sections. Section I have introduction part while in section II and section III we describe the previous work related to CEPAL circuit and design approach of CEPAL based NAND, NOR and XOR gates respectively. The proposed 1 bit CEPAL full adder is described in section IV. Section V and section VI presents results & discussion and conclusion respectively.

II. Previous Work

The structure and operation of CEPAL circuit are described in [1]. The basic structure of a CEPAL circuit and simulated waveforms of CEPAL inverter are shown in Fig. 1. CEPAL is composed of two charging pMOS diodes (P1 and P2), a pull-up (P-) network, two discharging nMOS diodes (N1 and N2) and a pull down (N-) network. Two sinusoidal supply clocks in complementary phases (i.e. PC and $\overline{PC}$) are used. Assume that initially output (Vout) is LOW, and the P-network is on while the N-network is off then the output either follows PC or its complement as it swings HIGH. Once Vout becomes HIGH the followed power clock then swings down and output node of CEPAL becomes floating but this situation is soon removed because at the same time the complement of the followed power clock swings up, thereby eliminating the weak HIGH at the output node.

Similarly the weak LOW at the output can be eliminated by the complementary energy paths. CEPAL have two more diodes in comparison to quasi static energy recovery logic (QSERL) [3], but power dissipation due to these additional diodes is not very large as there is only one charging or discharging transistor turned on at an instant of time. Thus QSERL and CEPAL circuits have similar power consumption however considerable improvements in area and power overheads can be achieved in CEPAL because a keeper in practice is necessary for QSERL circuits to avoid erroneous operation during hold phase.

III. Design Approach of CEPAL NAND, NOR, & XOR Gates

The NAND and NOR gates are universal gates and they can be used to design complex digital circuits. Exclusive-OR

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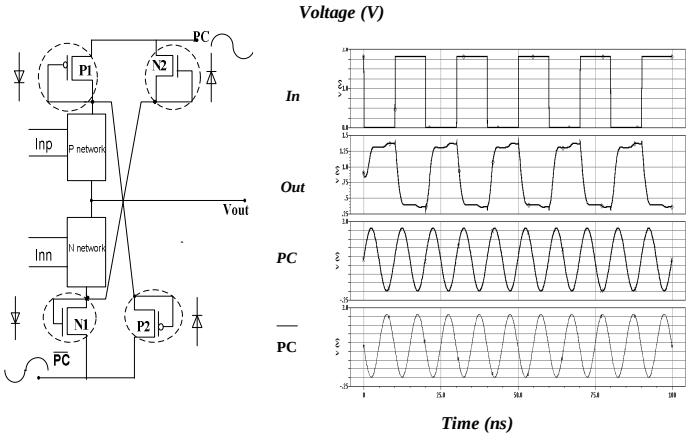
(XOR) gates are well known for their roles in larger circuits such as full adders and parity checkers. Therefore an optimized design of the XOR gates can certainly benefit the performance of the larger circuits.



(a) (b)

Fig. 1 CEPAL circuit (a) Circuit diagram (b) Simulation waveform of CEPAL inverter

The experimental work consists of simulating the circuit shown in Fig. 2(a), Fig. 3(a) and Fig. 4(a) using VIRTUOSO SPECTRE simulator of cadence with all the transistors of equal sizes of W/L= 0.24µm/0.18µm. The supply voltage, power clock frequency (f_{PC}), input frequency (f_{in}) and load capacitance are 1.8V, 100MHz, 50MHz and 10fF respectively.

A. CEPAL NAND Gate

The structure of CEPAL NAND gate is shown in Fig. 2(a). It consists of two p-channel MOSFETs (P1 and P2 connected in parallel) and two pMOS diodes D1 and D2 in the charging path. Similarly in the discharging path we have two n-channel MOSFETs (N1 and N2 connected in series) and two nMOS diodes D3 and D4. Supply voltages are two complementary sinusoidal power clocks (PC) and $\overline{(PC)}$.CEPAL AND gate can be realised by connecting the output of NAND gate to the input of a CEPAL inverter. Output logic levels in all CEPAL gates will always be slightly lower than input logic levels due to the non adiabatic losses (such as V_t drop across the transistors).

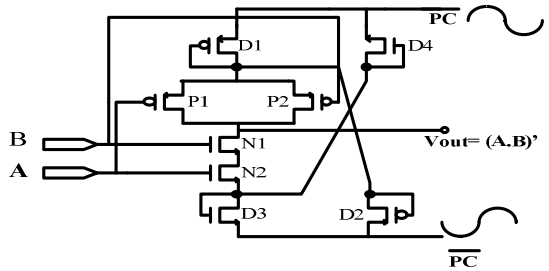


Fig. 2(a) CEPAL NAND gate schematic diagram

Fig. 2(b) shows the simulated timing waveforms which verifies the correct NAND/AND gate logic function

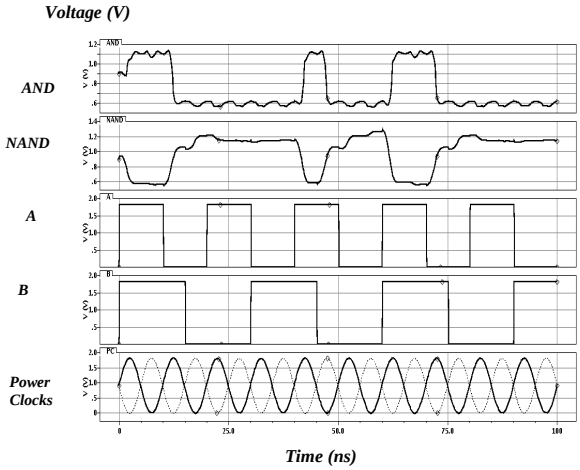


Fig. 2(b) Simulated CEPAL NAND gate timing waveforms

B. CEPAL NOR Gate

The structure of CEPAL NOR gate is shown in Fig. 3(a). It has two p-channel MOSFETs (P1 and P2 connected in series) and two pMOS diodes D1 and D2 for charging the load capacitance by supply clock PC. Two nMOS transistors N1 and N2 (connected in parallel) and two nMOS diodes are used for energy recovery to the power clocks. CEPAL OR gate is realised by connecting NOR gate output to the input of a CEPAL inverter.

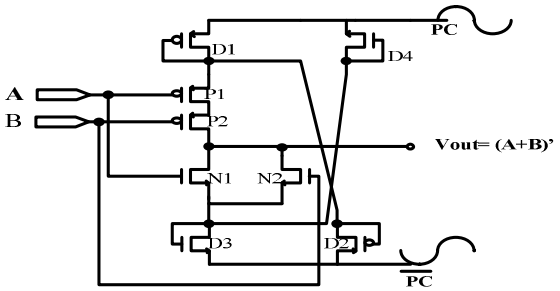


Fig. 3(a) CEPAL NOR gate schematic diagram

Fig. 3(b) shows the simulated timing waveform which verifies the correct NOR/OR gate logic function.

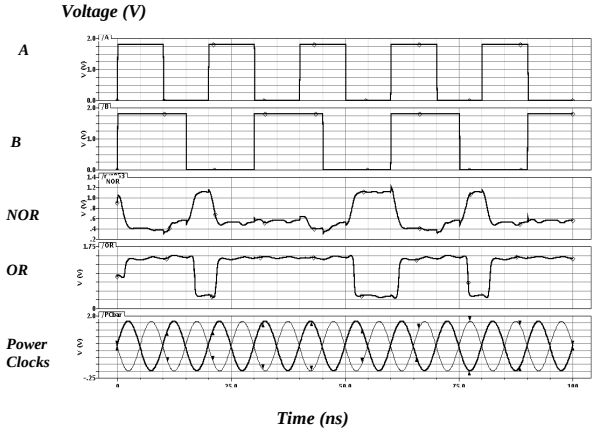


Fig. 3(b) Simulated CEPAL NOR gate timing waveform

C. CEPAL XOR Gate

The structure of CEPAL XOR gate circuit is shown in Fig. 4(a). This circuit consists of 4 pMOS transistors (P1-P4) and two diodes (D1&D2) in the charging path to the capacitive load and 4 nMOS transistors (N1-N4) and two nMOS diodes (D3&D4) in the discharging path.

A CEPAL NOT gate is also simulated with identical circuit parameters as used in other gates (like NAND/NOR etc.) and its simulated waveform is shown in Fig. 1(b).

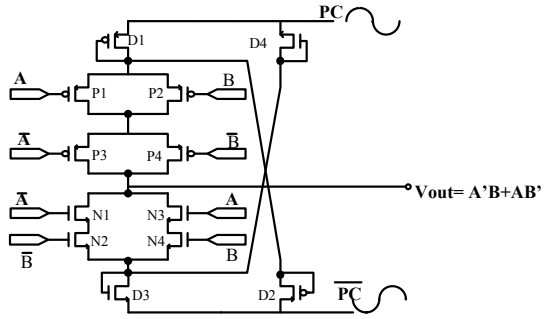


Fig. 4(a) CEPAL XOR gate schematic diagram

Fig. 4(b) consists of simulated timing waveform to verify the correct XOR gate logic function

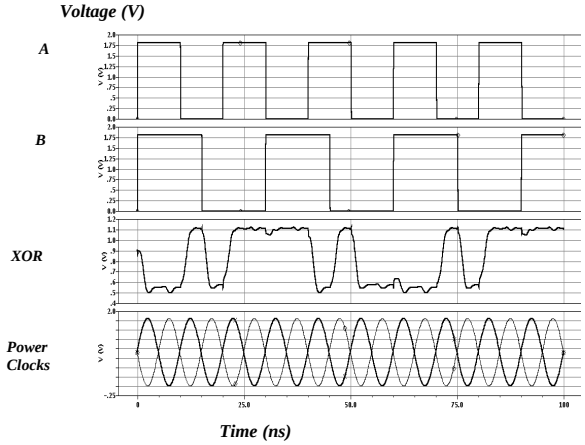


Fig. 4(b) CEPAL XOR gate simulated timing waveforms

For comparing the performance of CEPAL gates with the CMOS gates, CMOS NAND, NOR, XOR and NOT (inverter) gates are also simulated with identical circuit parameters and the calculated values of energy dissipation, power dissipation and delay for one cycle of charging and discharging are shown in Table I.

It may be observed that all the adiabatic gates have lesser power and approximately similar energy dissipation with a slight increased delay in comparison to the CMOS gates.

TABLE I
COMPARISON OF CEPAL& SIMILAR CMOS IN REPRESENTATIVE GATES FOR 1 CYCLE OF CHARGING & DISCHARGING AT f_{in}=50 MHz,f_{pc}=100MHz,C_L=10fF

Name of the circuit	Energy Dissipation (fJ)		Power Dissipation (μW)		Delay (ns)	
	CEPAL	CMOS	CEPAL	CMOS	CEPAL	CMOS
NAND gate	0.252	0.079	0.212	0.433	1.19	*0.183*
NOR gate	0.096	0.087	0.079	0.385	1.21	*0.226*
XOR gate	0.034	0.218	0.032	0.644	1.07	*0.339*
NOT gate	1.22	0.054	0.2	0.370	6.1	0.147

IV. PROPOSED CEPAL FULL ADDER CIRCUIT

A. CEPAL Half Adder

CEPAL half adder has been designed by taking one XOR gate and one AND gate together. The XOR gate is designed in Fig. 4(a). The AND gate is realized by connecting output of a NAND gate as an input to the inverter. The output of XOR gate is named as SUM1 and output of AND gate is CARRY1. A block level diagram of CEPAL half adder is shown in Fig. 5(a).

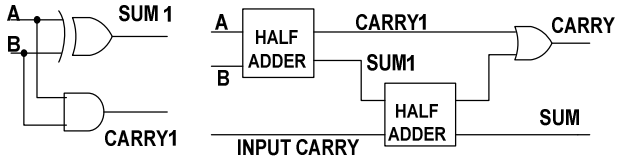


Fig. 5 Block level diagram of (a) CEPAL half adder (b) CEPAL full adder

B. CEPAL Full Adder

Using the half adder as a block, a full adder circuit is designed as shown in Fig. 5(b). The CEPAL full adder consists of two CEPAL half adders and an OR gate. The proposed CEPAL full adder & half adder and CMOS full & half adder have the same frequency ratio of input to PCs (i.e. 1/2) and equal switching probability of input for being HIGH and LOW. The width and length of all the MOSFETs were 0.24μm and 0.18μm respectively.

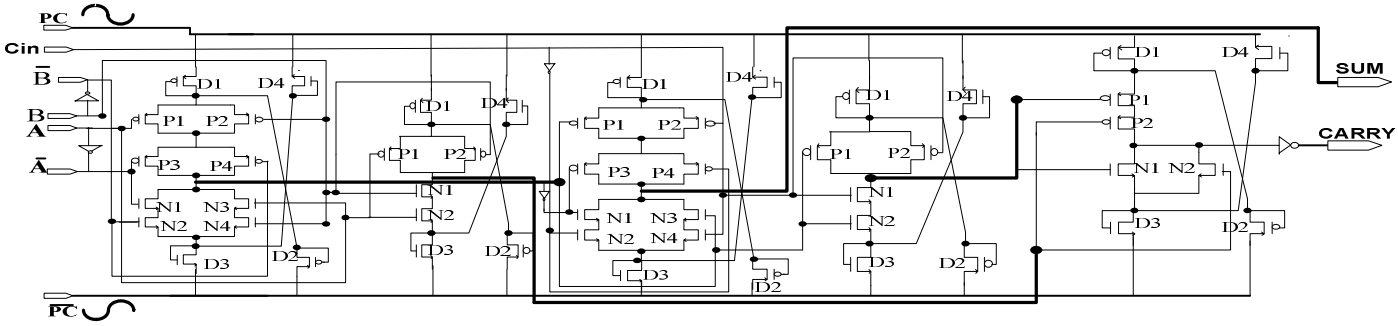


Fig. 6 Schematic of the proposed 1 bit CEPAL full adder circuit

V. Results and Discussion

In this section, we examine the functionality of our proposed 1 bit CEPAL adders and compare the results with the CMOS full adders. The simulations were performed using a VIRTUOSO SPECTRE simulator of cadence in 0.18µm UMC technology. The supply voltage, power clock frequency (f_{PC}), input frequency (f_{in}) and load capacitance used are 1.8V, 100MHz, 50MHz and 10fF respectively. Fig. 7(a) shows the simulation waveform of a CEPAL half adder. The combination of inputs are given as a strings A='11001100110011001100', B= '11100011100011100011'. The outputs namely SUM 1 and CARRY 1 are obtained in the form of a strings '00101111010000101111' and'11000000100011000000' respectively. Output logic levels are ('1'=1.34, '0'=0.3).

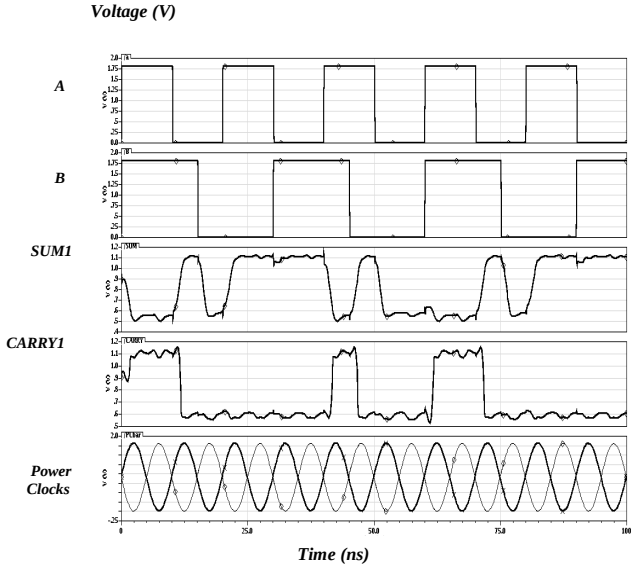


Fig. 7(a) Simulation waveforms of CEPAL half adder

SUM and CARRY waveforms for the input strings of A='11001100110011001100', B='11100011100011100011' and input carry= '11110000111100001111' are '11011111101100100000'and '11100000110011001111' respectively. Output logic levels are ('1'=1.54 & '0'=0.3). Full adder function is verified by the simulated outputs.

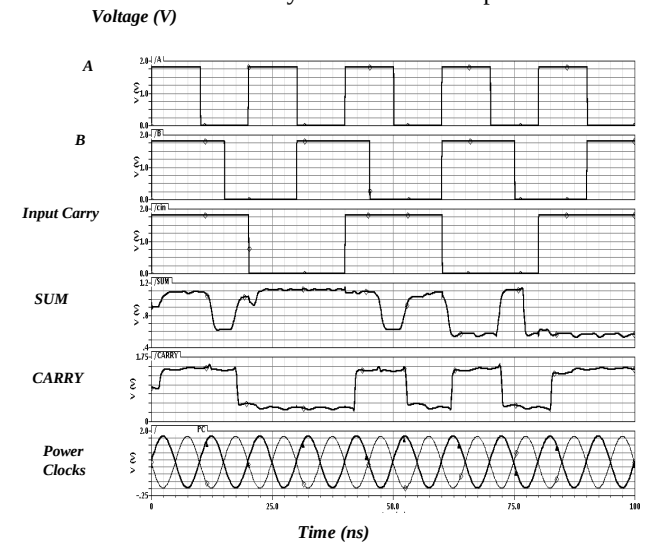


Fig. 7(b) Simulation waveforms of CEPAL full adder

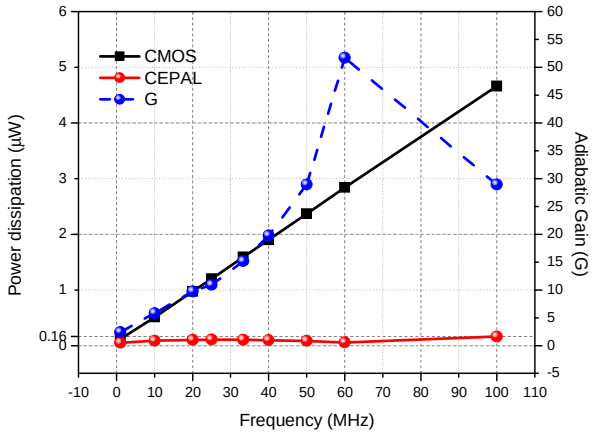


Fig. 8 Power dissipation per cycle and adiabatic gain versus operating frequency (at f_{PC}/f_{in}=2, V_{DD}=1.8V and C_L=10fF)

Adiabatic Gain 'G' is defined as the ratio between the energy dissipated by a traditional CMOS gate and the equivalent adiabatic gate. Higher adiabatic gain shows better energy efficiency.

The variation of adiabatic gain with different parameters (f_{in}, C_L & V) for full adder circuit is shown in Fig 8, Fig 9 and Fig 10 respectively.

Power dissipation of a full adder (CEPAL and CMOS) with the change in operating frequency from 1 MHz to 100 MHz is shown in Fig. 8. It is observed that CEPAL based full adder have lesser power dissipation than the static CMOS full adder at all frequencies and as frequency increases the power dissipation in CEPAL adder also increases because of increased resistance of the MOSFETs but still it is lower than the static CMOS full adder. Adiabatic gain is very high around 60MHz. Since in traditional CMOS gate energy dissipation does not depend on frequency while this relationship is linear for an adiabatic gate thus adiabatic gain decreases as frequency increases beyond 60 MHz .However, it should be noted that the contribution due to leakage, becomes predominant at low frequencies and due to this fact an unpredictable increasing adiabatic gain with frequency is observed at lower frequency ranges (up to 60MHz).

Power dissipation and adiabatic gain variation with load capacitance for a full adder (CEPAL and CMOS) is shown in Fig. 9. Since the energy dependence on load capacitance is parabolic in the adiabatic case and linear in a traditional CMOS circuit, the power dissipation increases rapidly with the load capacitance in CEPAL full adder circuit while this increase is small in CMOS full adder but still CMOS full adder have larger power dissipation than CEPAL full adder. Adiabatic gain increases with the load capacitance which shows the better driving capability of proposed adder circuit.

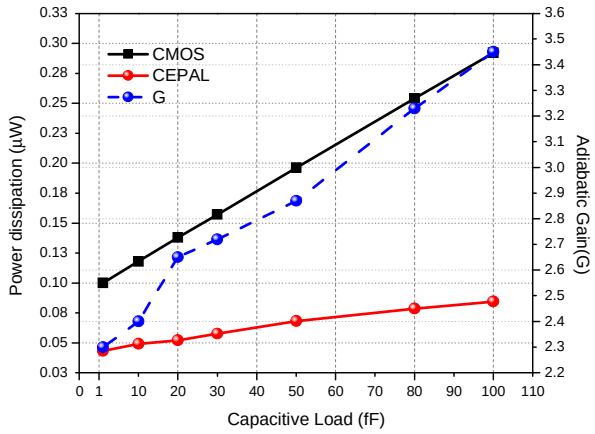


Fig. 9 Power dissipation per cycle and adiabatic gain versus load capacitance (at f_{PC}=2MHz, f_{in}=1MHz and V_{DD}=1.8V)

Fig. 10 shows the power dissipation and adabatic gain as a function of power supply voltage (V_{DD}). When power clock voltage increases the power dissipation increases with the square of V_{DD}, thus keeping V_{DD} very small may be a good choice for lesser power loss. But it is observed that as the power supply voltage is reduced from a certain value (in Fig. 10 below 1.2 V) at a particular opereating frequency (in Fig. 10 at 1MHz) output logic levels are incorrect and full adder logic function is not satisfied. The adiabatic gain decreases as the peak power clock votage increases, because output logic levels (hence power dissipation) increases with the power supply voltage.

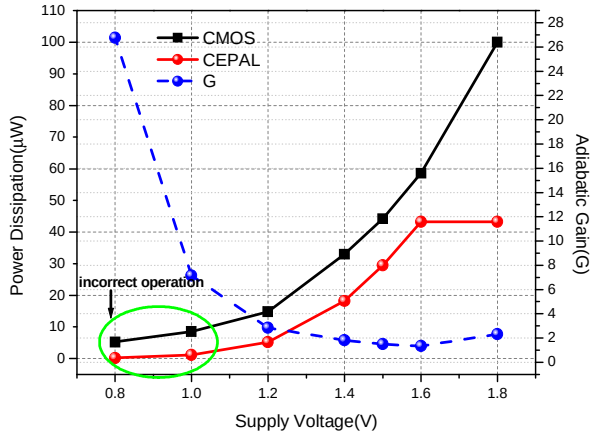


Fig. 10 Power dissipation per cycle and adiabatic gain versus peak power clock voltage (at f_{PC}=2MHz, f_{in}=1MHz and C_L=1fF).

From the above discussion it may be concluded that CEPAL full adder shows good power efficiency in wide operating conditions.

The comparison of a CEPAL and CMOS adders with similar circuit parameters has been shown in Table 2. It is observed that CEPAL based half adder exhibits a power saving of up to 92% with a slight increase in delay (4 nano seconds) to the CMOS half adder but this increased delay can be traded off because here performance is dominated by low power. Whereas it is also discovered that the energy levels of both CMOS and CEPAL half adders are nearly same.

The power and energy dissipation by a CEPAL full adder is reduced up to 96% and 70% respectively to the CMOS full adder. There is a small increase in delay of 3.2 nano-seconds which can be traded off with low power.

TABLE II
COMPARISON OF CEPAL AND SIMILAR CMOS IN REPRESENTATIVE ADDERS FOR ONE CYCLE OF CHARGING AND DISCHARGING AT f_{in}=50 MHZ ,f_{pc}=100MHZ, V_{DD}=1.8V, AND C_L=10fF

Name of the circuit	Energy Dissipation (fJ)		Power dissipation (µW)		Delay (ns)	
	CEPAL	CMOS	CEPAL	CMOS	CEPAL	CMOS
Half adder	0.405	0.408	0.093	1.22	4.35	0.335
Full adder	0.30	1.03	0.082	2.37	3.66	0.436

The layout of a CEPAL inverter circuit has also been drawn as shown in Fig. 11. From the layout it has been characterized that the chip area of a CEPAL ineverter is slightly higher than the CMOS circuit due to the four extra MOSFET diodes. CEPAL inverter has 41.23µm^2 adiabatic area while CMOS inverter have 14.54µm^2. Since inveter is the basic cell for any full adder circuit hence it can be generalized intitutively that a CEPAL full adder circuit may have a small increased area compared to CMOS full adder.

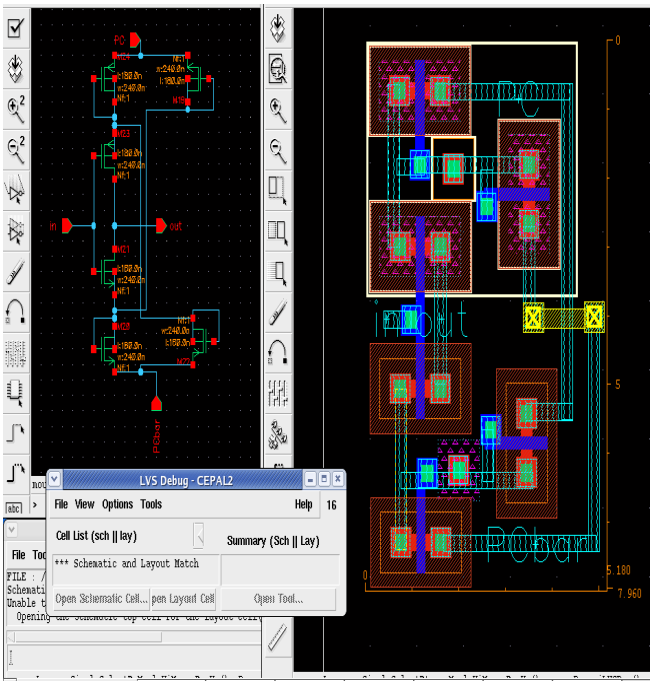


Fig. 11 Layout of a CEPAL inverter circuit

VI. CONCLUSION

In this paper we have presented a CEPAL full adder circuit and its performance with different parameter variation have been evaluated in terms of power dissipation. It is concluded

that CEPAL based full adder circuit consumes 70% lesser energy with a very small incremented area and delay compared to conventional CMOS full adder circuit at 100MHz frequency. The presented circuit has low on chip power density and thus it can be used in power aware high-performance VLSI circuitry.

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