World Academy of Science, Engineering and Technology
International Journal of Electrical and Computer Engineering
Vol:6, No:9, 2012

A 1.8 V RF CMOS Active Inductor with 0.18 um CMOS Technology

Siavash Heydarzadeh, Massoud Dousti

***Abstract*—**A active inductor in CMOS techonology with a supply voltage of 1.8V is presented. The value of the inductance L can be in the range from 0.12nH to 0.25nH in high frequency(HF). The proposed active inductor is designed in TSMC 0.18-um CMOS technology. The power dissipation of this inductor can retain constant at all operating frequency bands and consume around 20mW from 1.8V power supply. Inductors designed by integrated circuit occupy much smaller area, for this reason,attracted researchers attention for more than decade. In this design we used Advanced Designed System (ADS) for simulating cicuit.

***Keywords*—**CMOS active inductor , 0.18um CMOS technology , ADS

I. Introduction

COMS active inductors have found increasing applications in areas where an inductive characteristic is required. These applications include LC oscillators,RF bandpass filters,RF phase shifters,RF power dividers and ultra wideband low noise amplifiers [1]. Although the performance of monolithic integrated inductors in CMOS process has enjoyed a great progress, the large space occupied by the spiral inductors and the conductive substrate, has made passive inductors an improbable option to be employed in designing high-frequency circuit in which the use of multiple inductors is requisite[2]. An active inductor typically occupies 1-5% of the silicon area of a passive inductor. Some disadvantages of using active inductors, compared to spiral inductors that limit their use in RFIC and MMIC designs,are higher noise, nonlinear behavior , power dissipation, sensitivity to process, and voltage and temperature variations [3]. The active inductor presented here provides high value, least area occupation,insensitive to temperature and low power consumption.

II. Active Inductor Circuits

Researchers have introduced different kinds of circuits for active inductors. Some of these circuits are showen in Fig. 1,Fig. 2 and Fig. 3 [4],[5],[6]. The value of small-signal equivalent elements are obtained with equations (1) to (7).

For figure one:

$$C1 = C_{gs1} \tag{1}$$

$$R1 = \frac{1}{g_{o2}} \| \frac{1}{g_{m1}} \approx \frac{1}{g_{m1}}$$

$$R2 \approx \frac{g_{o1}}{g_{m1}.g_{m2}}$$

$$L1 = \frac{C_{gs2} + C_{gd2} + C_{gd1}}{g_{m1}.g_{m2}}$$

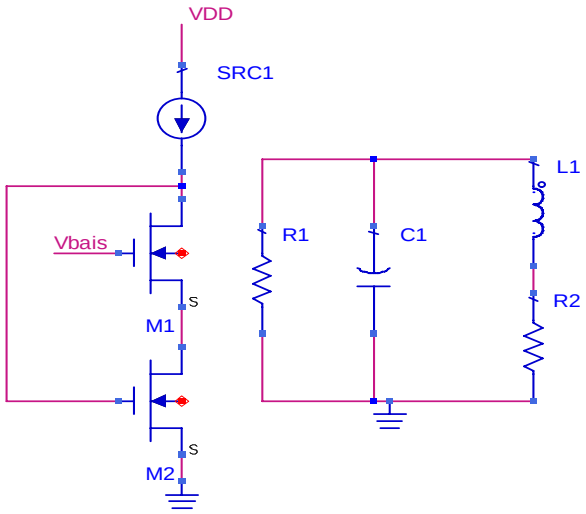

Fig. 1 Active inductor and small-signal equivalent

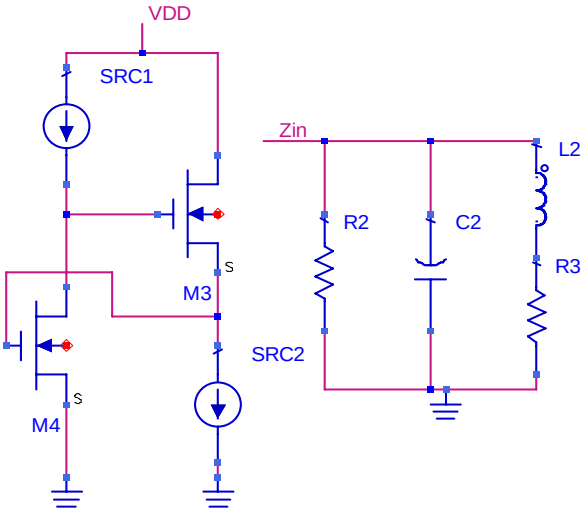

Fig. 2 Simple active inductor and equivalent circuit

S. Heydarzaded is with Science and research branch, Islamic Azad university,Tehran,Iran.(www.srbiau.ac.ir)

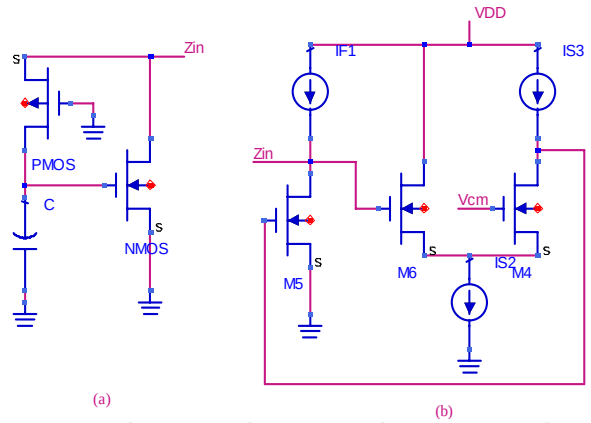

Fig. 3 (a) - Adan active inductor circuit (b)-Xiao active inductor circuit

For figure two:

$$R2 = \frac{1}{g_{ds3} + g_{m4}} \approx \frac{1}{g_{m4}} \quad (5)$$

$$L \approx \frac{Cgs3}{g_{m4}.g_{m3}} \quad (6)$$

For figure three (a):

$$Zin \approx \frac{SC}{g_{mp}.g_{mn}} \quad (7)$$

III. Active Inductor Specification

From among these active inductor circuits, figure one is selected and illustrated. The active inductor in Fig.1, as compared to other topologies, could use biasing current more proficiently. Because of using shunt feedback at the input node,the impedance is low where frequency is low. When the frequency is high enough, the gate-source capacitance will result in the drop of the feedback loop gain, the input impedance will raise with frequency. Simple structure and low noise are the most important advantages of this circuit. The active inductor in Fig.1 can work better in high frequency as compared to Fig.2 [7].Figure 4 shows the complete circuit of inductor that simulated.

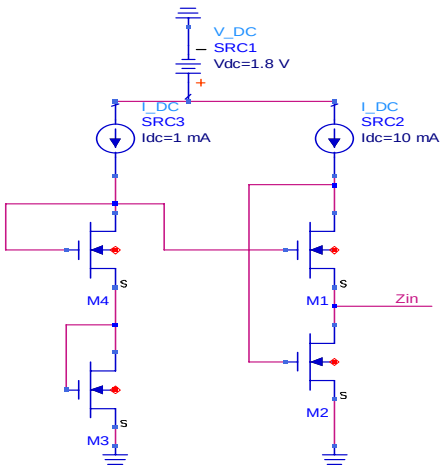

Fig. 4 The complete circuit of active inductor

Table I is presented transistors dimensions which utilized in active inductor circuit (Fig.4).

TABLE I
TRANSISTORS DIMENSIONS

PS	L (µm)	W (µm)	AD (pm)	AS (pm)	PD (µm)	(µm)
M1-M2	0.18	250	120	120	501	501
M3-M4	0.25	600	288	288	1201	1201

AD: drain diffusion area
AS: source diffusion area
PD: Perimeter of the drain junction
PS: perimeter of the source junction

$$AD = AS \cong W \times Ls \quad (8)$$

$$PD = PS \cong 2W + 2Ls \quad (9)$$

Ls in equation (8) , (9) depends on technology . For 0.18U COMS process Ls=0.48um. Ls is 0.55um for 0.13U CMOS process.

IV. Simulation Results

Table II shows the important parameters of taransistors which related to bais. These parameters determine the value of inductor (L) as we mention above.

TABLE II
TANSISTORS PARAMETERS

	g_m (mv)	V_{gs} (mv)	V_{ds} (mv)	I_d (mA)	$V_{ds,sat}$ (mv)	V_{th} (mv)	region
M1	80	667	367	10	130	503	sat
M2	57	600	232	5.3	104	495	sat
M3	20	462	462	1	57	499	sat
M4	20	437	437	1	57	473	sat

The numbers in Table II, have obtained from ADS report. Figure 5 shows the imaginary part of input impedance (imag(Zin)). The frequency range of simulation is included 1GHz to 6 GHz.

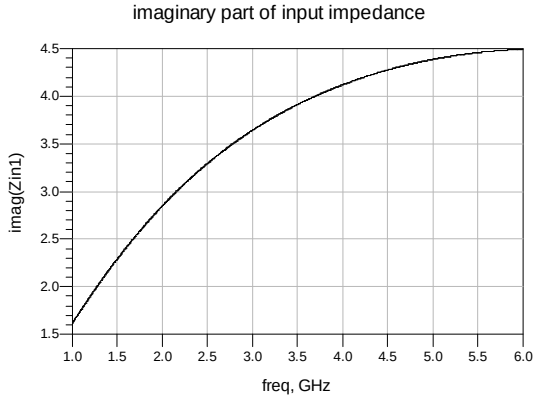

Fig. 5 Imaginary part of input impedance(imag(Zin)).

Input impedance smith chart is shown in Fig.6. Figure 7 represents the real part of input impedance (real(Zin))which is

related to dissipation resistance (R2 in Fig.1). S11 parameter is displayed in Fig. 8 .

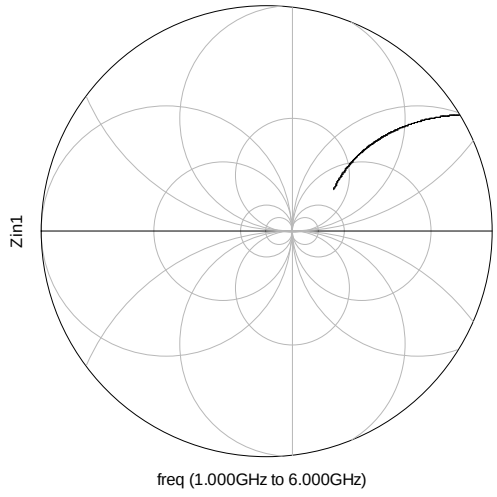

Fig. 6 Input impedance(Zin)

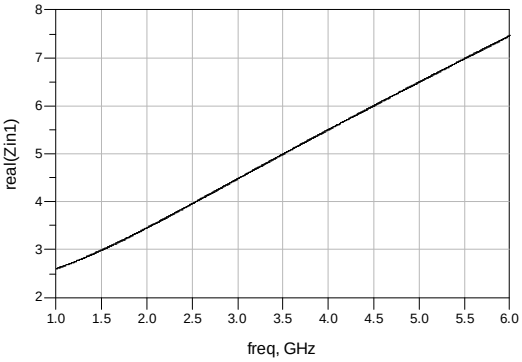

Fig. 7 real part of input impedance(real(Zin))

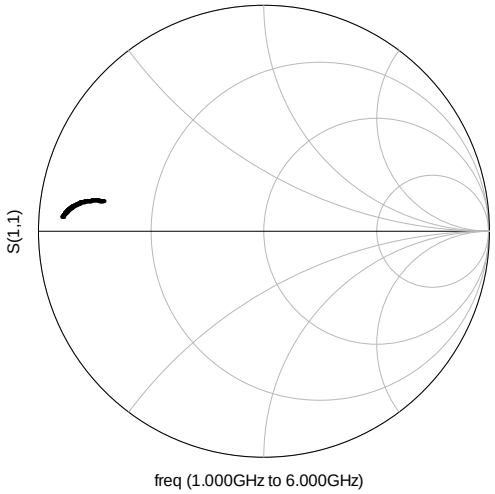

Fig. 8 S11 parameter after simulating cicuit

$$g_m = \sqrt{2.K'.Id.\left(\frac{w}{l}\right)} \tag{10}$$

According to equation (4) and (10):

$$L \propto \frac{1}{g_{m1}.g_{m2}} \tag{11}$$

$$gm1, gm2 \propto \sqrt{Id1.Id2} \tag{12}$$

$$L \propto \frac{1}{\sqrt{Id1.Id2}} \tag{13}$$

Figure 9 displays the effect of temperature on drain source currents (Temperature VS $1/\sqrt{Id1.Id2}$).This figure represents that temperature changing won't effect on inductor value(L).

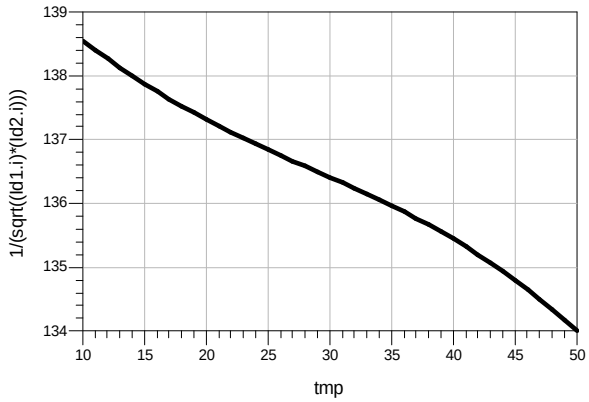

Fig. 9 Temperature effect on drain source currents

Inductor value (L) which obtained from equation (14) is displayed in Fig.10 .

$$\text{imag(Zin)} = 2\pi f L \rightarrow L = \frac{\text{imag(Zin)}}{2\pi f} \tag{14}$$

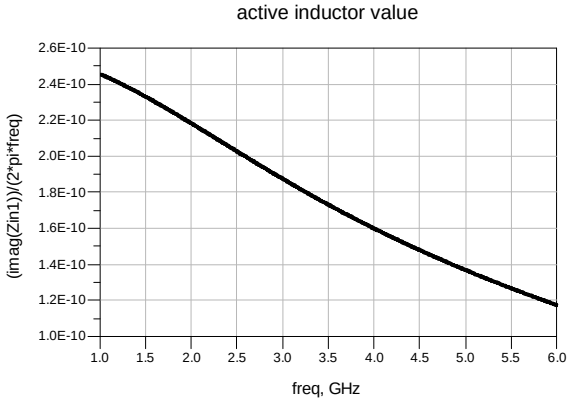

Fig. 10 Active inductor value (L)

Active inductance layout shows in figure 11. Using cadence software and 0.18um CMOS technology to produce this layout. The least area consumption are utilized.

V. Conclusion

A 0.18 um CMOS active inductor with 0.12nH to 0.25nH value in high frequancy was presented. The design has the capability of independent inductance value in different temperature. It consumes less than 20mW power form 1.8V power supply. The active inductor simulated in this paper had less than 8Ω loss resistance as Fig.7 showed. We used TSMC RF 0.18 um CMOS technology in simulating.

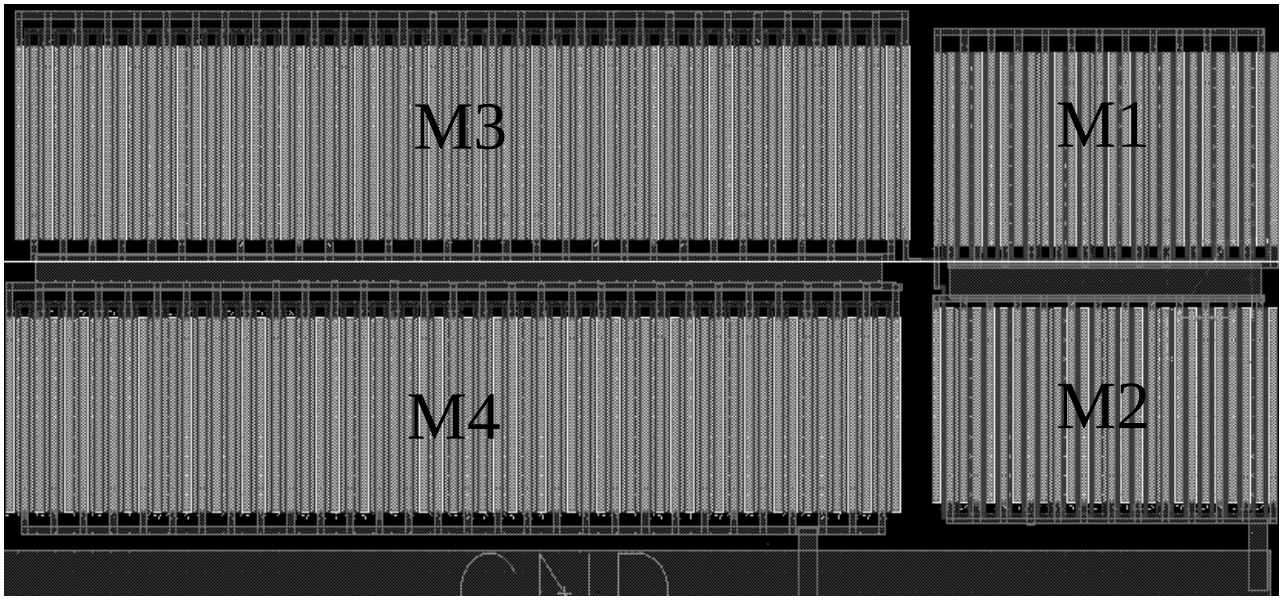

Fig. 11 Active inductance cadence layout with 0.18um technology

ACKNOWLEDGMENT

The authors thank M,jafari panah and H.G Darvish for their help.

REFERENCES

[1] M.Ebrahimzadeh, "A Low Voltage High Quality Factor Floating Gate Tunable Active Inductor with Independent Inductance and Quality Factor Tuning", International Journal of Computer an Electrica Engineering, Vol. 3, No. 2, April, 2011,1793-8163.

[2] M.Sabaghi,M.Rahnama,M.N.Lahiji,M.S.Miri,Sh.Rezakhani, "Design And Simulation of Differential Active Inductor With 0.18 um CMOS Technology", Canadian journal on Electrical and Electronics Engineering, Vol. 2, No. 9, September 2011.

[3] M.Ebrahimzadeh, "A Low Voltage, High Quality Factor Floating Gate Tunable Active Inductor with Independent Inductance and Quality Factor Tuning", International Journal of Computer an Electrica Engineering, Vol. 3, No. 2, April, 2011,1793-8163.

[4] H.Xiao,"Recent Integrated Active Inductor Patents",Recent Patent on Electrical Engineering 2009, 2, 182-186, Received: March 26, 2009; Accepted: July 17, 2009; Revised: August 20, 2009.

[5] M.Ebrahimzadeh, "A Low Voltage, High Quality Factor Floatin Gate Tunable Active Inductor with Independent Inductance and Quality Factor Tuning", International Journal of Computer an Electrica Engineering, Vol. 3, No. 2, April, 2011,1793-8163.

[6] M.J.Wu,Y.H.Lee,Y.Y.Huang,Y.M.Mu.J.T.Yang, "A CMOS Multi-Band Low Noise Amplifier Using High-Q Active Inductors", INTERNATIONAL JOURNAL OF CIRCUITS, SYSTEMS AND SIGNAL PROCESSING , Issue 2, Vol. 1, 2007.

[7] M.Sabaghi,M.Rahnama,M.N.Lahiji,M.S.Miri,Sh.Rezakhani, "Design and simulation of differential active inductor With 0.18 um CMOS Technology", Canadian journal on Electrical and Electronics Engineering Vol. 2 , No. 9, September 2011.

[8] C.leifso, J.W.Haslett, J.G. McRory, "Monolithic tunable active Inductor with independent Q control" ,IEEE Transactions on Microwave Theory and Techniques, vol. 48, no.6,Jan,2000, pp. 1024-1029.

[9] T. Soorapanth ,S. Wong, "A 0 dB il 2140 +_30 MHz Bandpass Filter Utilizing Q-enhanced Spiral Inductors in Standard CMOS" ,IEEE J. Solid-State Circuits, vol. 35, May, 2002 ,pp. 579–586.

[10] J. Savoj,B.Razavi,"High-Speed CMOS Circuits for Optical Receivers ",Norwood, MA: Kluwer, pp. 16–19,2001.

[11] G.Retz, H.Shanan, K.Mulvaney, P.Quinlan, "A Highly Integrated Low-power 2.4GHz Transceiver Using A Direct-conversion Diversity Receiver in 0.18μm CMOS" , IEEE 802.15.4 WPAN,IEEE Solid-State Cir Conf 2009,414-415a.

[12] C. Andriesei, L. Goras , " IMPROVED RF CMOS ACTIVE INDUCTOR WITH HIGH SELF RESONANT FREQUENCY",Author manuscript, published in 2010 IEEE International Conference on Electronics, Circuits and Systems, Athens, Greece ,2010.

[13] F. Yuan, "CMOS Active Inductors and Transformers Principle,Implementation, and Applications", New York,Springer, 2008.

Siavash Heydarzadeh was born in Tehran,Iran,in 1988.He received B.S degree in electronic engineering from Tafresh university,Tafresh,Iran,in 2011 . M.S university student in Science and research branch,Islamic Azad university,Tehran,Iran. He has several papers in the field of Electronic.His principle research interests include amplifier,active inductance ,active filter,RF application.S Heydarzadeh is a member of Young researchers club,Science and research branch,Islamic Azad university,Tehran,Iran.
Siavash136725@yahoo.com,S.Heydarzadeh@srbiau.ac.ir