Improvement in Silicon on Insulator Devices using Strained Si/SiGe Technology for High Performance in RF Integrated Circuits

Morteza Fathipour, Samira Omidbakhsh, Kimia Khodayari

Abstract—RF performance of SOI CMOS device has attracted significant amount of interest recently. In order to improve RF parameters, Strained Si/Relaxed $Si_{0.8}Ge_{0.2}$ investigated as a replacement for Si technology .Enhancement of carrier mobility associated with strain engineering makes Strained Si a promising candidate for improving RF performance of CMOS technology. From the simulation, the cut-off frequency is estimated to be 224 GHZ, whereas in SOI at similar bias is about 188 GHZ. Therefore, Strained Si exhibits 19% improvement in cut-off frequency over similar Si counterpart. In this paper, I_{on}/I_{off} ratio is studied as one of the key parameters in logic and digital application. Strained Si/SiGe demonstrates better I_{on}/I_{off} characteristic than SOI, in similar channel length of 100 nm.Another important key analog figures of merit such as Early Voltage (V_{EA}) ,transconductance vs drain current (g_m /I_{ds}) are studied. They introduce the efficiency of the devices to convert dc power into ac frequency.

Keywords—cut-off frequency, RF application, Silicon on insulator, Strained Si/SiGe on insulator.

I. INTRODUCTION

METAL - Oxide-Semiconductor-Filed-Effect-Transistor device has been the predominant technology during the past 35 years in microelectronic industry. The basic idea of MOSFET scaling is the progressive reduction of MOSFET dimensions, which results in higher packing density, higher switching speed and lower power dissipation of integrated circuits. Single gate SOI MOSFET has many benefits over traditional bulk MOSFET including high speed and low power and has proved useful for digital circuit design application.

SOI MOSFET is also wildly recognized as one of the most promising devices because of its short channel effect immunity reduction in leakage current and more scaling potential.

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In addition to digital circuits, these MOSFET devices will be strong contenders also for analog RF applications in the wireless communications market. Therefore, electrical characteristic improvement in such devices has attracted much attention.

In order to achieve higher drive current for better RF performance, Strained Si/SiGe is purposed. $Si_{1-x}Ge_x$-on-insulator (SGOI) is a very promising technology as it combines the benefits of two advanced technologies.

One of the drawbacks in Strained Si/SiGe technology is attributed to low thermal conductivity of Si_xGe_{1-x}. Low thermal conductivity is considered as a problem because of hot electron channel which increases operating temperature of integrated circuits. High temperature decreases carrier mobility due to lattice scattering. This effect makes the mobility improvement meaningless. The thermal conductivity of $Si_{0.8}Ge_{0.2}$ is about 5.1 $Wm^{-1}k^{-1}$,while thermal conductivity of Si is 148 $Wm^{-1}k^{-1}$and that of Ge is 60 $Wm^{-1}k^{-1}$.To alleviate the existing problem in Strained Si/SiGe technology, the Si_xGe_{1-x} layer thickness is considered to be very thin(<20nm) [1].

II. SIMULATION

In this section, the SiGe-on-insulator (SGOI) structure will be explained. Fig. 1 shows results of the simulation for SiGe-on-insulator (SGOI) device. The channel length material for strained-Si device is 100 nm.

The lattice constants for Si , Ge and Si0.8Ge0.2 are 5.431, 5.658 and 5.596, respectively. As an epitaxial layer grows on lattice-mismatched films, the difference in lattice parameter is accommodated elastically up to a certain critical thickness so that in-plane lattice parameter of the pseudomorphic film is equivalent to substrate .The elastic energy due to strain in the films increases with film thickness. When this thickness and elastic-strain energy rises above the critical value, the introduction of misfit dislocation becomes energetically favorable and the epilayer relaxes plastically.

The minimum value of film thickness is referred to as critical thickness. Strained Si film thickness is considered 7 nm , This is located on top of the 20 nm thick relaxed SiGe layer. The percent of the Ge mole fraction in SiGe layer (x %) controls the value of strain in the channel. Ge content of SiGe layer is 20%.The channel and source/drain Concentration are 1.0e17 cm-3 and 6.0e21 cm, respectively. Channel length is

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100 nm. Doping Concentration in both channel and source/drain is uniform. 2D analysis was carried out using SILVACO-ATLAS software [2] The simulations have been performed with Stress model to consider strain in Si .and dt.cbet for tunneling from conduction band to conduction band.
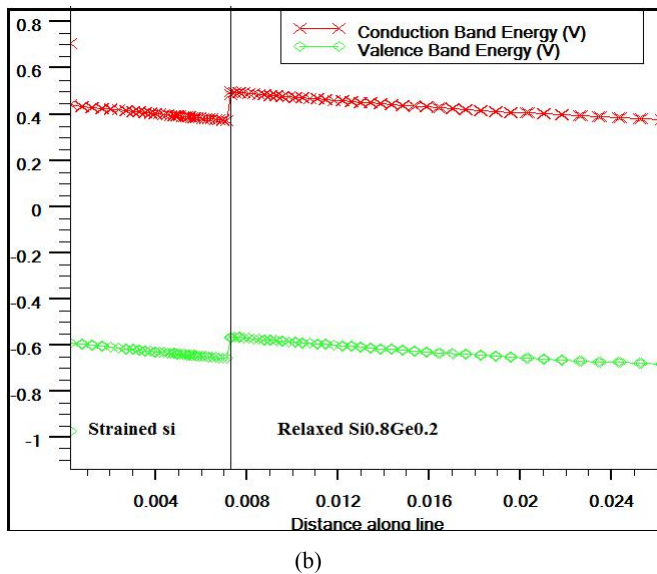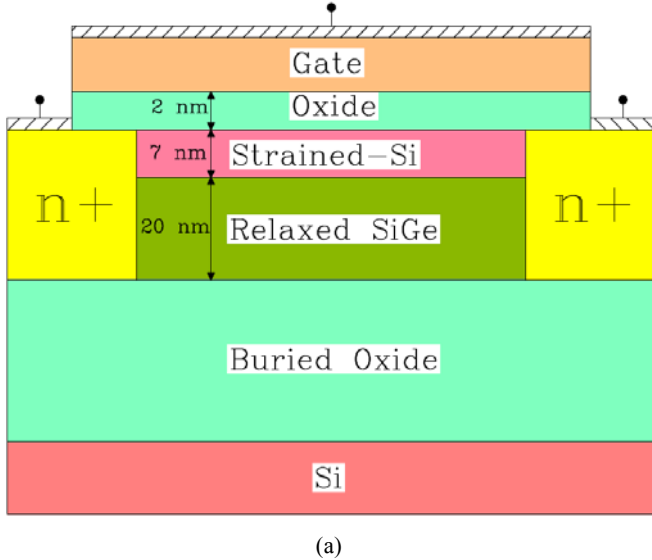
(a)

(b)

Fig. 1 (a) Cross section of the strained-Si/SiGe-on-Insulator.
(b) Energy band diagram of strained Si/SiGe-on-Insulator along depth at Vgs=0 V

III. DC ANALYSIS

When Si is grown pseudomorphically on relaxed SiGe which has a larger in-plane lattice constant than bulk Si, the strain splits the six-fold degeneracy of the Si conduction band minimum, resulting in a conduction band offset between strained Si and Si-Ge, and increases electron mobility due to lower in-plane effective mass and reduced intervalley scattering [3]. Electron mobility enhancement increases drive current in Strained Si/SiGe OI in comparison with SOI .I_{on} has shown in fig.2 for both devices at V_{ds}=0.1 V. Strained Si/SiGe

OI demonstrated the significant improvement in 100 nm gate length. The result would be interesting for SOI higher performance logic and for SOI RF applications.
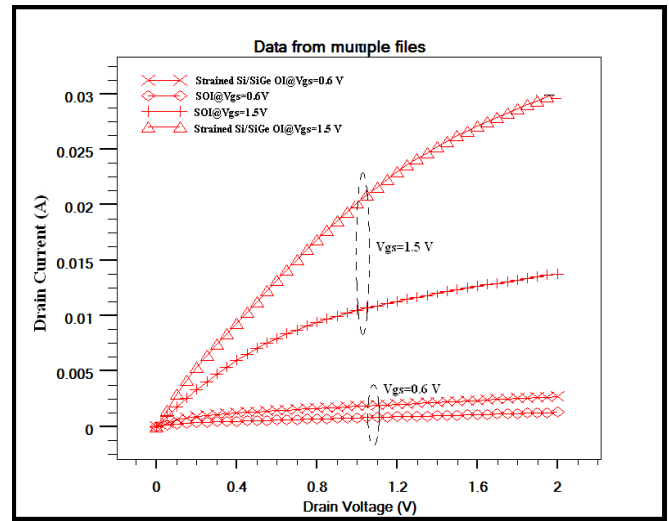

Fig. 2 Comparison of simulated ID-VD curves for strained Si/SiGe OI and SOI at Vgs=1.5 V, 0.6V

A. Threshold Voltage

I_D-V_G electrical characteristics for both SGOI and SOI have been presented in fig. 3. Comparing threshold voltage (V_t) of Strained Si with Unstrained Si , Strained Si shows slight degradation .Extracting that of V_t from simulation, threshold voltages for Strained Si/SiGe OI and SOI were found to be 0.41 V and 0.46 V, respectively. The lowered conduction band edge of strained Si and difference in energy band as well as electron affinity account for difference in threshold voltage. Strain boosts the electron affinity property of strained Si ,so the effective mass and energy band gap reduce in this device.
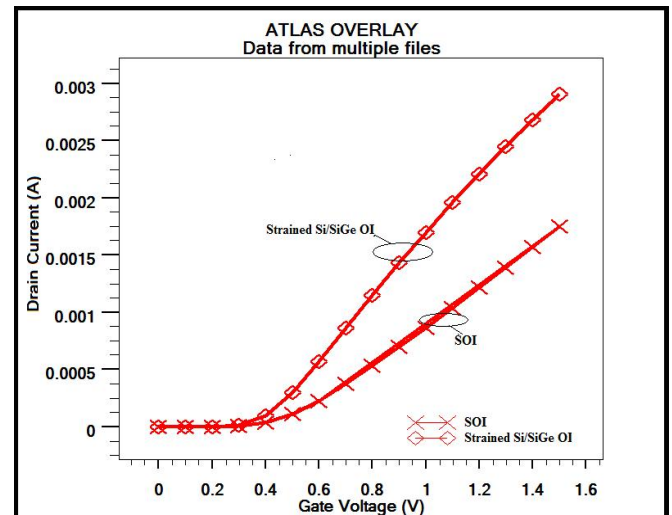

Fig. 3 Comparison of simulated I_D-V_G curves for strained Si/SiGe OI and SOI at Vgs=1.5 V, 0.6V

The V_t for the strained-Si nMOSFET is written from classical theory:

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$$V_t = \Phi_{MS} + \psi_s - Q_d / C_{ox}$$

Where, Φ_{MS} is the gate-body work-function difference, Qd is the depletion charge density, ψ_S is the surface potential at the strong inversion and C_{ox} is the gate-oxide capacitance [4]. In Strained Si device, Φ_{MS} and ψ_s are lower due to the band offset, So the threshold voltage is reduced.

B. Sub-threshold Conduction

Sub-threshold current is an important factor in digital application design. Sub-threshold or weak inversion conduction current occurs when $|V_G| < |V_t|$. In weak inversion, a small amount of inversion charge is always present in the channel. The weak conduction in channel is called leakage current As presented. in Fig. 4, the leakage current for SOI is smaller than strained Si/SiGe OI. The junction leakage increases in strained device. Small band gap in $Si_{0.8}Ge_{0.2}$ increase, 5-6 times, the saturation current of reverse diode in comparison with that of traditional Silicon mosfet. Although the leakage current increases in strained Si, I_{on}/I_{off} rises. Higher drive current in strained channel enhances this ratio
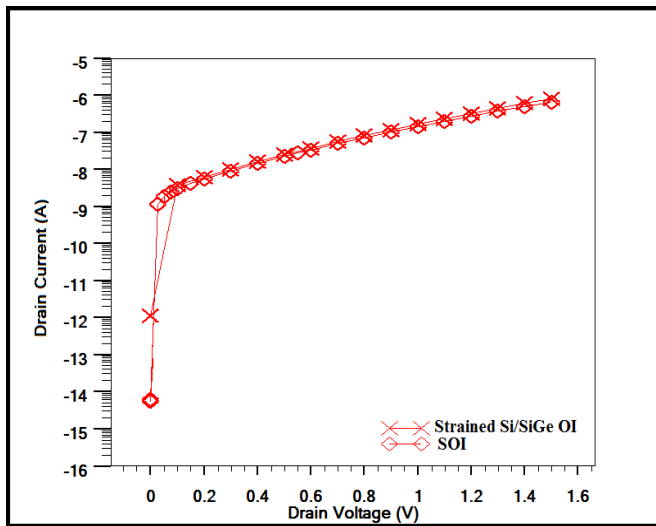

Fig. 4 Leakage current curves for strained Si/SiGe OI and SOI at Vgs=0 V

Sub-threshold slope is a figure of merit of transistor performance and shows the rate of decrease of I_{off}. Fig. 6 shows the sub-threshold characteristics of Strained Si/SiGe OI and SOI at V_{ds}=0.1 V .Comparing sub-threshold conduction of Strained Si with Silicon device, Silicon device sub-threshold slope shows slight degradation.

C. Transconductance

The transconductance (g_m) of a MOSFET device is an important metric since it indicates the switching speed of the device. The plots in Fig. 7 compares the transconductance values for the strained-Si and conventional Si, respectively. It shows a peak transconductance enhancement of 100% in strained-Si device over conventional Si with similar dimensions. The higher transconductance obtained from

strained-Si SOI device indicate their suitability for use in high performance circuits and this would be better suited than the conventional Si devices in this type of application.
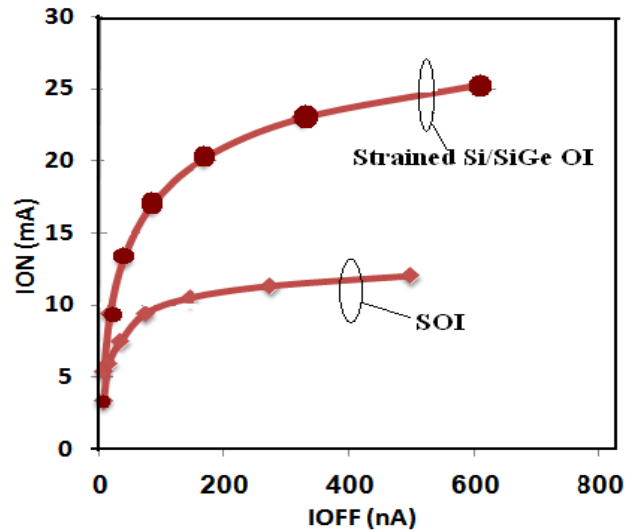

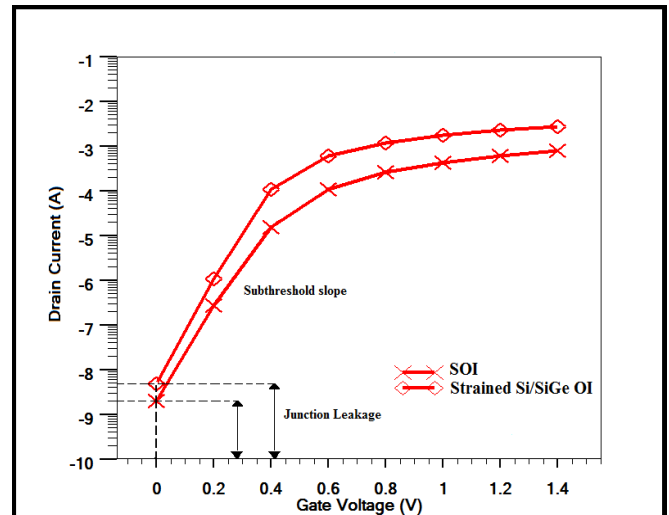Fig. 5 Comparison of I_{on}/I_{off} ratios for strained Si/SiGe OI and SOI

Fig. 6 subthreshold curves showing leakage current

Fig. 8 compares the transconductance versus drain current (g_m/I_{ds}) for the strained-Si and conventional Si . g_m/I_{ds} is the key analog performance of a technology .It shows the efficiency of the devices to convert dc power into ac frequency. The gm/Ids ratio does not depend on device dimensions and its value is inversely proportional to the channel inversion level. Low g_m/I_{ds} values correspond to strong inversion operation and its high values corresponding to weak inversion

IV. AC ANALYSIS

A. Output Conductance and Early Voltage

Simulation result shows the output conductance (g_{ds}) decreases for strained Si device. The output conductance is inversely proportional to early voltage $(V_{EA}=I_{ds}/g_{ds})$. Early

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voltage is a key factor in AC frequency circuit design[5]. Higher early voltage improves intrinsic voltage gain. Transconductance of strained Si/SiGe OI and SOI device with a gate length of 100 nm as a function of gate voltage

In proposed structure, in despite of increasing output conductance, the early voltage has been increased roughly. Higher drive current in strained channel compensate the reduction in output conductance.
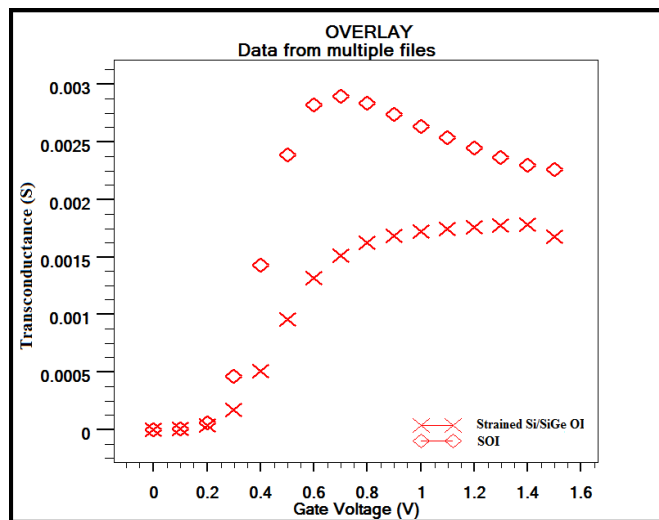

Fig. 7 Transconductance of strained Si/SiGe OI and SOI device with a gate length of 100 nm as a function of gate voltage
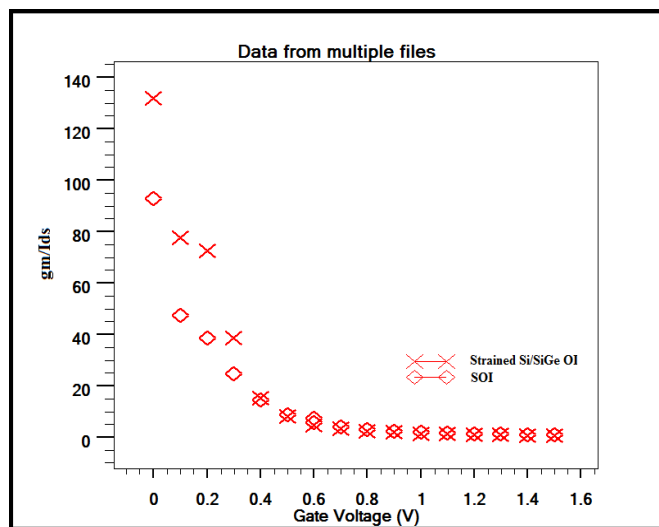

Fig. 8 Comparison of g_m/I_{ds} curves for strained Si/SiGe OI and SOI

B. Cut-off frequency

Cut-off frequency(f_t) was extracted as the frequency at which short circuit current gain (h21) is 0 db. Cut off frequencies for strained Si/SiGe OI and SOI are about 244 GHZ and 188 GHZ, respectively. Improvement in transconductance in strained channel device causes increase in cut off frequency $f_t=gm/(2\pi*C_{gg})$. The results were obtained for Vg=1.5 V.
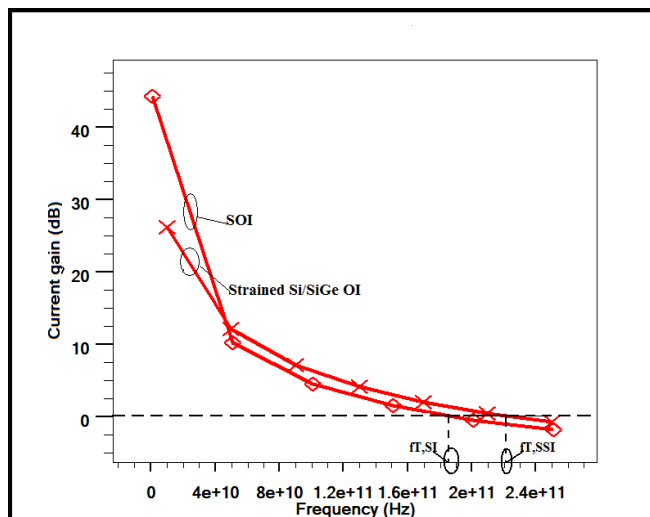

Fig. 9 F_t (was extracted as the frequency at which short circuit current gain (h21) is 0 Db) for strained Si/SiGe OI and SOI

V.CONCLUSION

Strained Si, due to its higher carrier mobility is considered as replacement for conventional silicon. The use of strained Si /SiGe material improves the speed performance of SOI device by offering higher electron mobility. Therefore the On-state current and transconductance will improve in strained Si/SiGe. The results show a peak transconductance enhancement of 100% in strained-Si device over conventional Si .

A significant improvement of about 19% in cut off frequency is achived.

Strained Si/SiGe device performance is enhanced through changes in material properties rather than changes in device geometry and doping. Therefore, strained Si is a promising candidate for improving the performance of Si CMOS technology .This structure is useful for low power analog and digital application

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