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A New True RMS-to-DC Converter in CMOS Technology

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***Abstract*—**This paper presents a new true RMS-to-DC converter circuit based on a square-root-domain squarer/divider. The circuit is designed by employing up-down translinear loop and using of MOSFET transistors that operate in strong inversion saturation region. The converter offer advantages of two-quadrant input current, low circuit complexity, low supply voltage (1.2V) and immunity from the body effect. The circuit has been simulated by HSPICE. The simulation results are seen to conform to the theoretical analysis and shows benefits of the proposed circuit.

***Keywords*—**Current-mode, squarer/divider, low-pass filter, converter, translinear loop, RMS-to-DC.

I. Introduction

THE RMS-to-DC converter as an electronic measuring circuit is employed for computing of the average energy content in an electronic signal. This converter is widely used in instrumentation devices [1] and biomedical ICs [2]. Recently some integrated forms of this converter have been proposed [3-7]. Some proposed design techniques are based on the bipolar dynamic translinear loop (TL) implementation [3]. However, in many situations, particularly in mixed A/D systems, it is desirable to implement the circuits in MOS technology. Up-down translinear loop (TL) [4] and class-AB linear transconductors [5], based on CMOS technology have been employed, too. The main drawback of these circuits are as follows: firstly; most of these circuits operate in one quadrant input current, so additional circuits for full-wave rectification is needed ; secondly, employing low supply voltage in these circuits restricts input dynamic range. Thirdly, the low pass filter for time-averaging operation requires a complex circuit with many transistors. Recently, this converter has been designed based FG-MOS transistors that operate in either square-root-domain [6] or log-domain [7]. However, in these techniques, large capacitors at the floating gate of transistors take large chip area. Furthermore, removing of residual charge trapped at the floating gate during fabrication process require complex technology [8]. Therefore, it is expected that their realization will take high cost. In this work, to overcome the above problems, a new RMS-to-DC converter based on a squarer/divider is presented. The circuit uses MOS transistors that operate in strong inversion and works in two-quadrant input, so the full-wave rectifier is not required. For the time average operation, a simplified current-mode low pass filter using one capacitor and one MOS transistor is employed [6].

The paper organized as follows. In section 2, the basic principle of current mode true RMS-to-DC converter operation is discussed. Circuit design is presented in section 3. Simulation results of the proposed RMS-to-DC converter are described in section 4 and in section 5 the conclusion is provided.

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II. Basic principle

The definition of the root mean square value of a signal with a period of T is given by:

$$I_{out} = \sqrt{\frac{1}{T}\int_{t}^{t+T} I_{in}^2(t)dt} \qquad (1)$$

where $I_{in}(t)$ and $I_{out}(t)$ are input and output currents of the RMS-to-DC converter, respectively.

A mathematically equivalent expression, but more precise considering the offset of the system, is given by [3]:

$$I_{out} = \left\langle \frac{I_{in}^2(t)}{I_{out}} \right\rangle \qquad (2)$$

where $\langle ... \rangle$ represents the averaging operation.

The block diagram of proposed converter is shown in Fig.1, in which it consists of a squarer/divider and a low pass filter.

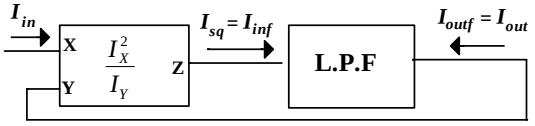


Fig. 1: Block diagram of the RMS-to-DC converter [3]

III. Circuit design

A. Two-quadrant squarer/divider

In CMOS technology, the squarer/divider has been carried out by using of MOS translinear [4, 9, 10], or class AB transconductance circuits [5]. The stacked loop [9] similar to class AB transconductance [5] suffers from body effect. In the electronically simulated loop, additional circuitry is needed to force the two averages of the gate-source voltages of the loop be equal [10]. In [4], for implementation of the converter, up-down translinear loop is employed. However, in the these proposals, all of above proposed squarer/divider circuits

operate in only one quadrant input current, so additional circuits for full-wave rectification of the input current is needed. Fig. 2 shows the basic circuit of the MOS up-down translinear loop, which is formed by transistors M1, M2, M3 and M4 that assumed all are operating in saturation region. Using Kerchief voltage rule (KVL) for gate-source voltage of these four transistors that are connected in series will obtain:

$$V_{gs1} + V_{gs2} = V_{gs3} + V_{gs4} \tag{3}$$

In other side, the drain current of MOS transistor that operates in strong inversion is given by:

$$I_{ds} = \frac{\beta}{2}\left(V_{gs} - V_t\right)^2 \tag{4}$$

where V_{gs} is the gate-source voltage of transistor, V_{th} is the threshold voltage, β stands for transconductance parameter. It should be pointed out that, in this analysis the channel-length modulation effect will not be considered. Despite this, the negligible influence of these effects in the circuit will become apparent in the simulation results of the circuit.

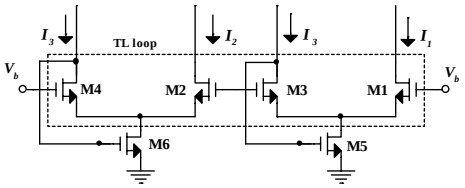


Fig. 2 Basic circuit diagram of the translinear loop

Considering equal aspect ratio for transistors of TL, and also equal injected current for transistors M3 and M4, substituting (4) into (3) it results:

$$\sqrt{I_1} + \sqrt{I_2} = \sqrt{4I_3} \tag{5}$$

In other side, the squarer/divider function can be introduced by:

$$I_{sq} = \frac{I_{in}^2}{I_{rms}} \tag{6}$$

where I_{in} is input current of squarer/divider, I_{rms} is the output current and $I_{rms}\left(=I_{out}\right)$ is the divisor.

Aiming to operate in two-quadrant operation at the input of squarer/divider, it can be shown that (6) can be expressed in square-root terms as [6]:

$$\sqrt{\frac{\left(\frac{I_{sq}}{2}+\frac{I_{rms}}{2}\right)+I_{in}}{2}} + \sqrt{\frac{\left(\frac{I_{sq}}{2}+\frac{I_{rms}}{2}\right)-I_{in}}{2}} = \sqrt{I_{rms}}\,. \tag{7}$$

Now, comparing (7) and (6) shows that, these two equations are equivalent by assumption that:

$$I_1 = \frac{I_{rms}}{4} + \frac{I_{in}}{2} + \frac{I_{in}^2}{4I_{rms}} \tag{8a}$$

$$I_2 = \frac{I_{rms}}{4} - \frac{I_{in}}{2} + \frac{I_{in}^2}{4I_{rms}} \tag{8b}$$

$$I_3 = \frac{I_{rms}}{4} \tag{8c}$$

Subtraction of (8a) and (8b) gives:

$$I_1 - I_2 = I_{in} \tag{9}$$

and summation of (8a) and (8b) gives, then using (6) it is obtained that:

$$I_{sq} = 2\left(I_1 + I_2 - 2I_3\right) \tag{10}$$

Fig.6 shows the complete circuit diagram of the proposed two-quadrant squarer/divider based on (9) and (10). A similar circuit diagram but with different analysis for the two-quadrant squarer/divider has been reported in [11]. In this circuit, transistors M1, M2, M3 and M4 form translinear loop. Transistors M2 and M8 (and also mirrored transistor M7) will split the input current I_{in} with respect to (9). It should be pointed out that, by changing the sign of I_{in} in (7) the result don't unchanged. So, the squarer/divider input operate in two-quadrant and full wave rectifier not needed. For preparation of the term $\left(I_1 + I_2\right)$ in RHS of (10) transistors M9 and M10 are employed, in which injected current in transistors M5 and M6 sample two summation currents $\left(I_1 + I_3\right)$ and $\left(I_2 + I_3\right)$, respectively; and then these two currents are mirrored and gathered in node A, by transistors M9 and M10, which will results:

$$I_{M9} + I_{M10} = I_1 + I_2 + 2I_3 \tag{11}$$

Substituting (11) into (10) and then using (8c), it will be concluded that:

$$I_{sq} = 2\left(I_{M9} + I_{M10} - 4I_3\right) \tag{12}$$

For preparation of (12), the term $4I_3$ is prepared by mirrored transistor M14 and subtracted from node A; and finally, output current of squarer/divider I_{sq} is obtained by employing current mirror transistors M15 and M16 by multiplying current by coefficient two.

As Fig. 3 shows, the minimum supply voltage of the circuit is one V_{gs} plus two V_{ds}, and since extra biasing current and voltage are not needed, the static power consumption is decreased. The input of the circuit can accept both positive and negative currents, so it operates in two-quadrant and full wave rectifier is not needed which lead to low circuit complexity.

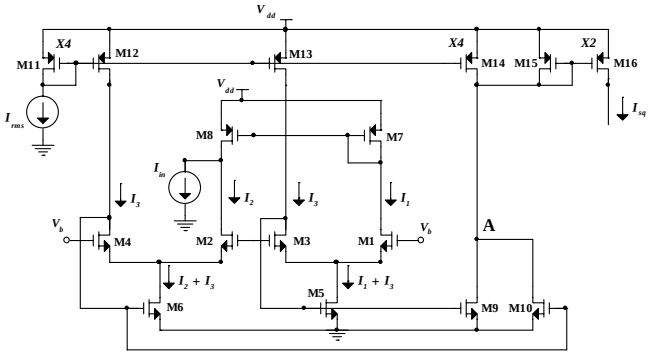


Fig. 3 Complete circuit diagram of the two-quadrant squarer/divider

B. Low pass filter

A first order low pass filter in current-mode can be represented in time domain as:

$$\frac{dI_{outf}}{dt} = \omega_c\left(I_{inf} - I_{outf}\right) \tag{13}$$

in which, ω_c is cutoff frequency, I_{inf} is input current of the filter and I_{outf} is output current of the filter.

Employing circuit of Fig. 4 and I-V relationship of transistor Mf1 that operate in saturation region, it can be shown by considering the filter cutoff frequency as following [6]:

$$\omega_c = \sqrt{\frac{2\beta I_{outf}}{C}} \tag{14}$$

for the input frequencies that are more than five times more than the cutoff frequency($\omega_{in} \geq 5\omega_c$), the accuracy of more than 1% is obtained [12], and it lead to [6]:

$$I_{cap} = I_{inf} - I_{outf} \tag{15}$$

Fig. 5 shows the simplified circuit diagram of the filter based on (15), which consist of just a transistor and a capacitor [6].
From (14), it can be concluded that the accuracy of more than 1% is achieved by proper choosing of capacitor value which is:

$$C \geq \frac{50\beta I_{true-RMS,max}}{\omega_{min}^2} \tag{16}$$

where ω_{min} is the lower end of the frequency range and $I_{true-RMS,max}$ is the higher end of the RMS of the input (output) current range.

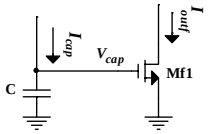


Fig. 4 Current-mode low-pass filter principle

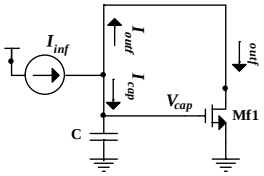


Fig. 5 Circuit diagram of the proposed current-mode low-pass filter [6]

IV. Simulation Results

Fig. 6 demonstrates the complete circuit diagram of the proposed RMS-to-DC converter, employing block diagram of Fig. 1 and circuit diagrams of Figs. 3 and 5. The circuit was simulated by Hspice with 0.18µm AMS CMOS process parameters. V_{dd}=1.2V, V_b=0.55V and C=300nF were used. Fig. 7 shows steady state time response of RMS-to-DC converter for 20uA peak-to-peak amplitude and 10kHz frequency sinusoidal and triangular input currents. Fig. 8 demonstrates the relative error of the converter output current for different amplitudes of the input currents. It can be seen in that the errors less than 3% are achieved for amplitudes between 2.5uA and 30uA. Simulation results shows that the power consumption of the circuit for the maximum accepted input current is less than 100uW. To provide more insight into the proposed technique, table I summarizes a comparison with formerly reported CMOS RMS-to-DC converters by showing some important parameters of the converters.

V. Conclusion

In this paper a new RMS-to-DC converter by the proposed squarer/divider and a simplified current-mode filter with low circuit complexity is designed. The square/divider circuit employs translinear loop and it features, low supply voltage and two-quadrant input. Also this circuit does not require extra bias current injection. Simulation results prove that the proposed design can be used for RMS measuring integrated circuit.

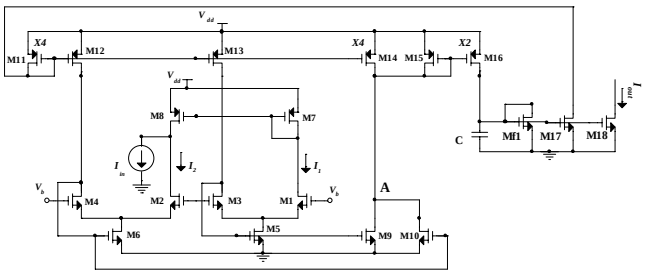
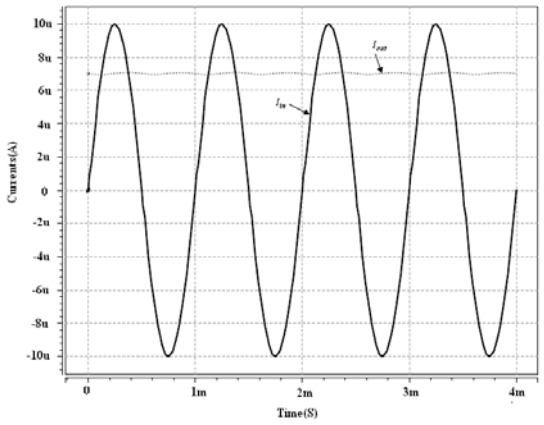
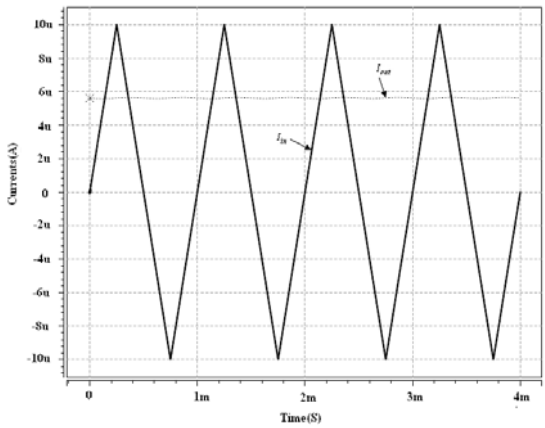


Fig. 6 Circuit diagram of the proposed RMS-to-DC converter



(a)



(b)

Fig. 7 Time response of the input current (dotted) and output current (solid) of the RMS-to-DC converter for a) sinusoidal input current b) triangular input current

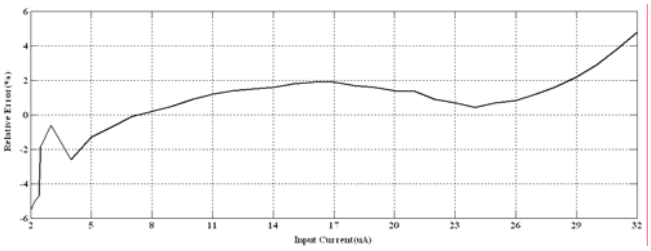


Fig. 8 Relative error versus input current of the RMS-to-DC converter

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TABLE I COMPARISON WITH FORMER RMS-TO-DC CONVERTERS

Parameter	Ref. [4]	Ref. [5]	Ref. [6]	Ref. [7]	This Work
Basic Principle	S.R.D. translinear	Class-AB Transconduc.	S.R.D. FG-MOS	Log-domain FG-MOS	MOS Trans linear loop
Technology	2.4u	0.5u	0.6u	0.35u	0.18u
Supply Voltage	1.5V	1.5V	1.2V	0.9V	1.2V
Circuit Complexity (Transistor no.)	108 MOS	40 MOS	1 FG-MOS + 14 MOS	6 FG-MOS + 7 MOS	18 MOS
Input Range	5uA-11uA @2%R.L.	12uA-22uA @3%R.L.	5uA-30uA @3%R.L.	0.6n-400nA @2%R.L.	2.5uA-30uA @3%R.L.
Operation Area of Input	1 Quad.	1 Quad.	2 Quad.	2 Quad.	2 Quad.