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Two New Low Power High Performance Full Adders with Minimum Gates

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***Abstract*—**with increasing circuits' complexity and demand to use portable devices, power consumption is one of the most important parameters these days. Full adders are the basic block of many circuits. Therefore reducing power consumption in full adders is very important in low power circuits. One of the most power-consuming modules in full adders is XOR/XNOR circuit. This paper presents two new full adders based on two new logic approaches. The proposed logic approaches use one XOR or XNOR gate to implement a full adder cell. Therefore, delay and power will be decreased. Using two new approaches and two XOR and XNOR gates, two new full adders have been implemented in this paper. Simulations are carried out by HSPICE in 0.18µm bulk technology with 1.8V supply voltage. The results show that the ten-transistors proposed full adder has 12% less power consumption and is 5% faster in comparison to MB12T full adder. 9T is more efficient in area and is 24% better than similar 10T full adder in term of power consumption. The main drawback of the proposed circuits is output threshold loss problem**.**

***Keywords*—**Full adder, XNOR, Low power, High performance, Very Large Scale Integrated Circuit.

I. INTRODUCTION

WITH the continuously increasing chips' complexity and number of transistors, circuits' power consumption is growing as well. Technology trends show that circuit delay is scaling down by 30%, performance and transistor density are doubled approximately every two years, and the transistor's threshold voltage is reduced by almost 15% every generation. All of these technology trends lead to higher and higher power consumption in circuits. Higher power consumptions raises chips' temperature and directly affect battery life in portable devices as it causes more current to be withdrawn from the power supply. A higher temperature directly affects circuit operation and reliability; complicated cooling and packaging techniques are required. In addition, higher current density either shortens battery packs [1] .

Full adders are fundamental units in various circuits, especially in circuits used for performing arithmetic operations such as compressors, comparators, parity checkers and so on [2].

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There are several issues related to the full adders. Some of them are, power consumption, performance, area, noise immunity and regularity and good driving ability[3]. Several works have been done in order to decrease transistor count and consequently decrease power consumption and area [2,5,6,14]. Some of them has threshold loss problem that cause non-full swing outputs, low speed and low noise immunity. However, usually they have less power consumption in comparison to full adders with full swing outputs. Not full swing full adders are useful in building up larger circuits as multiple bit input adders and multipliers. One such established application is the Manchester Carry-look ahead Chain (MCC) [2][4].

There are two types of full adders in case of logic structure. First, is static style and second is dynamic style. Static full adders commonly are more reliable, simpler and lower power than dynamic ones. However, dynamic full adders are faster and some times more compact than static full adders. Dynamic full adders suffer from charge sharing, high power due to high switching activity, clock load and complexity. Many full adders are in dynamic style and static style. Some researchers combine these two structures and propose mixed dynamic static full adders.

In this paper, we propose two static 1-bit full adder cells based on two new logic approaches.

II. LOW POWER FULL ADDER DESIGN

There are several sources of power consumption in CMOS circuits.

1) Switching Power: Due to output switching during output transitions.
2) Short Circuit Power: Due to the current between VDD and GND during a transistor switching.
3) Static Power: Caused by leakage current and static current.

Researchers have been found many ways to reduce power consumption in CMOS full adder circuits. The summery are some considerations to design of full adders.

1) Output and input capacitances should be low to reduce dynamic power. Therefore, fewer nodes should be connected to SUM and COUT signals.
2) Avoid using inverters will reduce switching activity and static power.
3) Avoid using both VDD and GND simultaneously in circuit components. It can reduce short circuit and static power.
4) Using Pass transistors usually lead to low transistor count

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full adders with low power consumption. However, sometimes pass transistor full adders have not full swing outputs due to threshold loss problem. PMOS cannot pass logic 0 and NMOS cannot pass logic 1 completely. Uncompleted swing reduces dynamic power but sometimes increases leakage power, because transistors do not turn off completely by poor signals.

5) Most important components of the power consumption in full adders are the XOR and XNOR gates. Therefore, more work should be done to reduce transistor count and power of these components or completely omit them [6].
6) Reducing number of transistors usually lead to reduce the power in full adders. However, sometimes it does not improve PDP. Therefore, reducing transistor counts does not always lead to reduce in PDP or power consumption.

III. PREVIOUS WORKS REVIEW

All of the full adder circuits can be divided into two groups in point of output. The first group of full adders has full swing outputs. C-CMOS [9], TFA [9] , TGA [8], 14T [10], 16T [10] belong to the first group. The second group is the full adders without full swing outputs. These full adders usually have low number of transistor, less power consumption and less area occupation. The full adders of first group have good driving ability, high number of transistors, high area and usually higher power consumption in comparison to group two.

General form of the relationship between three inputs A, B and C with outputs SUM and Carry are in equation (1)

$$SUM = A \oplus B \oplus C \quad (1)$$
$$COUT = AB + C(A \oplus B)$$

These outputs can be expressed in many different logic expressions. Therefore, many full adder circuits can be designed using the different expressions. There are three main components to design a full adder cell[12]. Those are XOR or XNOR, Carry generator and SUM Generator. In[11] different components have been combined to make 41 new 10-transistor full adders. Each full adder that uses more than one logic style is called hybrid full adder [12]. Elgamel et. Al. in [12] categorizes hybrid-full adder cells into three groups. XOR-XOR, XNOR-XNOR and Centralized full adders. Group 1 and 2 are very similar together. We categorize hybrid full adders into two groups. Some of the full adders do not belong to any of these two groups such as MB12T [13].

A. Cascaded Output Full Adders

In This category signal SUM is generated using, either two cascaded XOR or two cascaded XNOR modules. Fig. 1 shows these two types of circuits. Almost all the circuits in this category suffer from high delay to generate SUM and COUT signals. As we will see later in simulation, the critical delay is to generate COUT signal in SERF circuit. Fig. 3 shows SERF full adder [5] that belongs to this category.

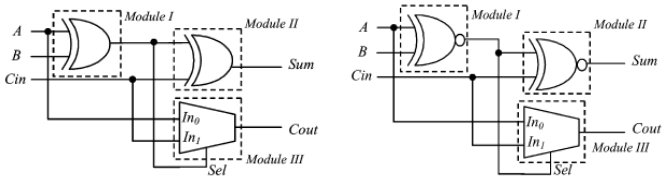


Fig.1 (a) group 1: cascaded full adder using two XOR gates [12]; (b) cascaded full adder using two XNOR gates[12].

B. Centralized Full Adders

In this category, COUT and SUM are generated using intermediate signals XOR and XNOR. In this group, output COUT and SUM is generated faster than the outputs in full adders of group 1. The key point here is to produce intermediate signals simultaneously. Otherwise, there may be glitches, unnecessary power consumption, and longer delay. Several works exist in the literature to produce simultaneous XOR-XNOR signals[15]. Fig. 2 shows the basic blocks of the second category. TGA and TFA are in this category.

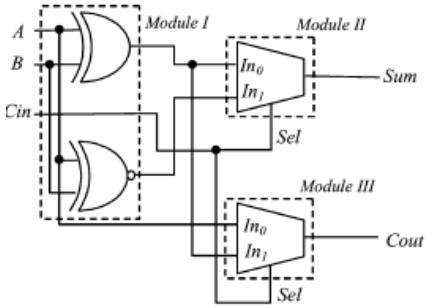


Fig. 2. Centralized full adder [12].

In this study, we chose well-known SERF, MUX-based and the full adder in [14], in order to comparison. We chose three non-full swing full adders, because both of our proposed designs are not full swing. We chose MUX based, because that is one of the fastest and lowest power design of the full adders. Many papers compared their design with SERF full adder cell. We used XOR module of [10] in one of our design, therefore it has been chosen to compare with the proposed designs. We study these three adders in continue.

SERF use energy recovery technique to decrease the power consumption. Energy recovery logics reuse charge. Therefore, it consumes less energy than the other full adders. Fig. 3 shows SERF full adder. This circuit is one of the best full adders in term of power consumption. There are some problems in this circuit. First SUM is generated from two-cascaded XNOR gates (group1) which lead to long delay. Second, it cannot work correctly in low voltage. As shown in Fig. 4 in the worst case, when *A=B='1'* there is $2V_{tn}$ threshold loss in output voltage. Therefore, logic 1 is becomes equal to $VDD\text{-}2V_{tn}$ in this case. The suitable operating supply voltage is limited to $VDD > 2V_{tn}+|V_{tp}|$. Second, there are five gate capacitances on node X. It causes to long delay in generating of intermediate $A \oplus B$ signal and finally delay in generating SUM and COUT. This problem also increases the power.

MBA12T uses 12 transistors. This full adder cell has been implemented based on six multiplexers. Each multiplexer is

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implemented in pass transistor logic design. Fig. 5(a) shows a simple multiplexer used in the MBA-12T. As shown in Fig. 5 (b) there are not any VDD or GND in this circuit. Therefore, power consumption has been decreased significantly. As can be seen in the Fig. 5(b) there are some paths containing three serried transistors. It causes to increase delay of producing SUM signal. The size of each transistor in mentioned path should be three times larger to balance the output and optimize the circuit for PDP. Therefore, the area of the circuit is increased.

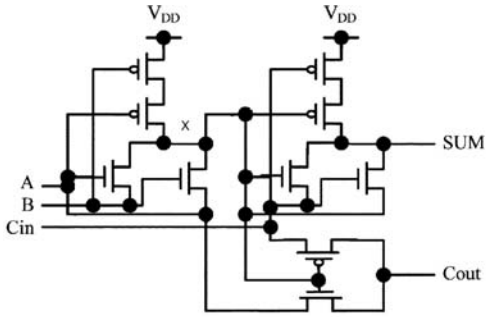


Fig. 3. SERF full adder circuit [5].

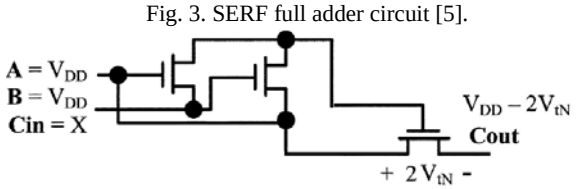


Fig. 4. Worst case of threshold loss problem in SERF full adder[13].

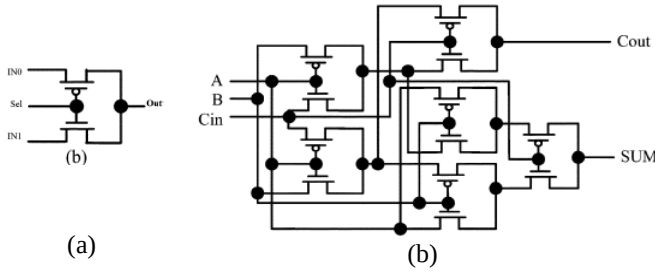


Fig. 5 (a). Multiplexer used in MBA12T; (b) MB12T full adder circuit [13].

In 10T [14] circuit, ten-transistor make a full adder in form of centralized structure. Intermediate XOR and XNOR are generated using three-transistor XOR and XNOR proposed by [7]. As shown in Fig. 6 SUM and COUT are generated using two double transistors multiplexers. 3T XOR and XNOR consume high energy due to short circuit current in ratio logic. Maximum serried transistors here are two transistors while in MB12T are three transistors.

Outputs have threshold loss problem due to non-full swing output of XNOR and XOR circuit and pass gate multiplexer output stage. By adjusting proper sizes for transistors, acceptable swing can be achieved. In term of intermediate nodes and capacitances, each XOR and XNOR circuits drives two gates. Input C drives two transistor gates.

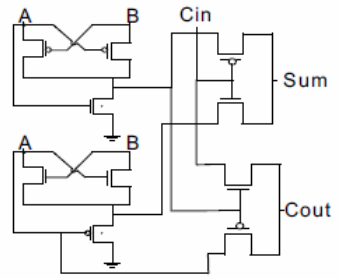
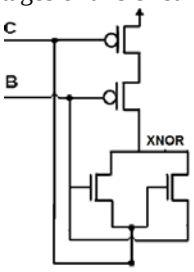


Fig. 6. 10T full adder use two three-transistor XOR-XNOR.

IV. Two XNOR and XOR Circuits Used in the Proposed Full Adders

A. Four Transistor XNOR Module

The circuit in Fig. 7 has been employed as XNOR circuit [2], in the one of the proposed full adders [10]. As Fig. 7 shows, this circuit has been implemented with pass gates in hybrid style. There are not any GND in this circuit. Therefore, static power consumption has been reduced. High speed NMOS transistors increase the speed of the circuit in three cases of inputs. When C=B=0, both NMOS transistors are off and PMOS block is on. Two PMOS transistors are serried together. Therefore, it leads to high delay to charge up the output. In the case that C=B=1, output has threshold loss problem and its voltage becomes equal to $VDD\text{-}V_T$. The main drawback of this XNOR is threshold loss problem. Low power consumption and low number of transistors are two advantages of this circuit.



CB	*OUT*
0 0	*VDD-V_T*
01	*GND*
1 0	*GND*
1 1	*VDD*

Fig. 7 The XNOR with four transistors.

B. 3T XOR Module

Fig. 8(a) shows the schematic of the XOR gate that we use in this paper to implement nine-transistor full adder[7]. The output states vs. input values are in Fig. 8 (b). In case of A equal to 1 and B equal to 0, output generates from a ratio logic. In this state high current is withdrawn from input A to GND that causes high power consumption and poor logic 1. However, by appropriate transistor sizing acceptable logic level is reachable.

V. Proposed Logic Approaches and Full Adders

In this section, two logic approaches to design low power high performance full adders are proposed. We propose two 1-bit full adder cells. The first full adder is implemented with 10 transistors and the second one with 9 transistors.

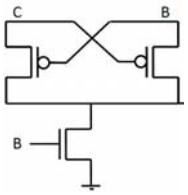
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A. Two Alternative Logic Approaches

As you can see in Table I, COUT and SUM can be produced using intermediate signal $B \oplus C$ or $\overline{B \oplus C}$. As shown in the Fig. 9 the proposed logic approach uses only one XOR or XNOR gate and two multiplexer to implement the Carry and SUM. XOR or XNOR gates are the most power hungry components of the full adder cells. Therefore, the new logic approach will reduce the power consumption.

CB	*OUT*
0 0	$\lvert V_{Tp} \rvert$
01	*VDD*
1 0	*Ratio*
1 1	*0V*

(a)

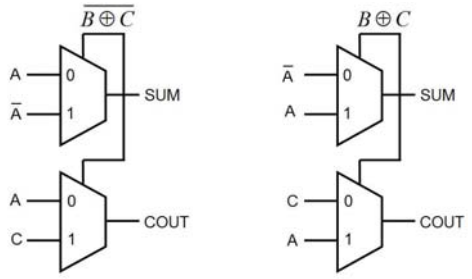


(b)

Fig. 8. (a) Truth table of the 3T XOR circuit. (b) 3T XOR circuit [14][7]

TABLE I
TRUTH TABLE FOR THE PROPOSED STRUCTURES

C	B	A	$B \oplus C$	$\overline{B \oplus C}$	COUT	SUM
0	0	0	0	1	C	A
0	0	1	0	1	C	A
0	1	0	1	0	A	$\overline{A}$
0	1	1	1	0	A	$\overline{A}$
1	0	0	1	0	A	$\overline{A}$
1	0	1	1	0	A	$\overline{A}$
1	1	0	0	1	C	A
1	1	1	0	1	C	A



(a) (b)

Fig. 9. (a) structure a. (b) structure b.

B. Static 10T Full adder (S10T)

In this circuit, we used the proposed logic approach of Fig. 9(a). We have only one XNOR gate. The four-transistor XNOR module has been used in this full adder. As can be seen in the Fig. 10, XNOR signal is used as the selector of two static multiplexer. XNOR signal has V_T threshold loss. Output multiplexers have V_T threshold loss too. Therefore, this circuit has threshold loss problem as well as SERF circuit. Intermediate signal XNOR drives two PMOS and two NMOS transistor gates. COUT and SUM generator circuits are two multiplexers that each uses only two transistors. There are not any VDD and GND in these components therefore these components consumes low power. Simplicity of the carry generator and sum generator circuits are another reason to decrease power and delay in these circuits. The main problem of the circuit is output threshold loss problem. The total number of transistors used in this circuit is ten. There is semi-inverter to invert input A. This inverter should work only when XNOR signal is equal to logic 0. Therefore, we use XNOR signal as GND of the inverter to decrease short circuit and leakage power in the inverter. On the other hand, switching activity on the node X will be reduced by using XNOR signal in the mentioned inverter. Input C, drive one transistor gate and two transistor junctions.

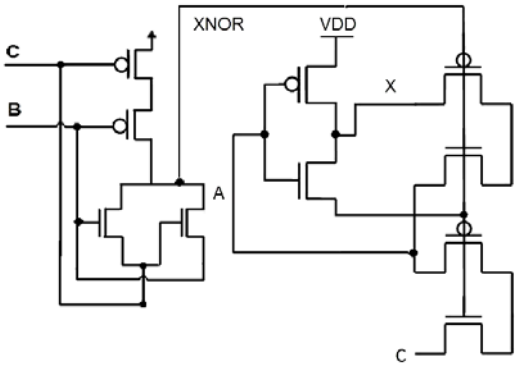


Fig. 10. S10T proposed full adder using structure a.

C. 9T Full Adder

In this design, we use three-transistor XOR module as shown in the Fig. 11 the difference between 9T and S10T is in the selector circuit of the output multiplexers. As mentioned earlier this XOR circuit has high power consumption due to static power consumption. Acceptable output swing for logic 1 in this circuit is the reason that we chose this circuit. We adjusted proper sizes for transistors to avoid high threshold loss in the XOR output and consequently outputs SUM and COUT. This full adder worked successfully in 1V supply voltage and 0.18µm technology. We used structure of Fig. 9 (b) to implement the nine-transistor full adder. Again, in order to reduce power we use XOR signal as the VDD of the input inverter in the path of signal A. The total number of transistors for this full adder is nine.

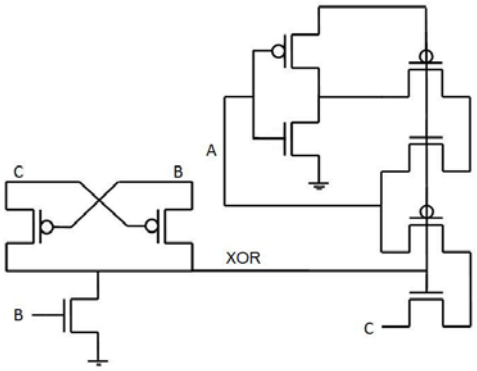


Fig. 11. 9T proposed full adder cell using structure b and 3T XOR.

VI. SIMULATION SETUP

All the netlists have been simulated using HSPICE in 0.18µm bulk technology. Output loads have been added according to Fig. 12. We used two inverters with same W/L to

make output buffers. Output load was added at input of the output buffers, to evaluate driving capability of the circuits without output buffers. We used buffers to check the output logic levels. Power and delay of inverters have been included in power and delay calculation of the whole circuit. The transistor sizes for buffers are two for PMOS and one for NMOS. A fixed value 1fF capacitance has been added at the output of the second inverter.

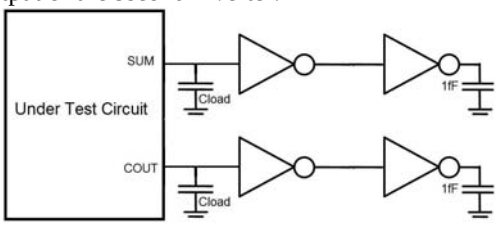


Fig. 12. Output buffers and loads.

Minimum output load for all the simulation is 2fF, except for the case, that we study the effect of output load on full adder. In that case, output load changes from 2fF to 500fF.

Theoretically, SERF and S10T cannot work correctly below 1.1V power supply. Therefore, to make comparison fair, we chose the 1.1V supply voltage as the minimum supply voltage of the simulation. Supply voltage is 1.8V for all simulations. We change the supply voltage from 1.1V to 1.8V to study the effects of supply voltage on the properties of the circuits. Normal frequency in the simulations is 200MHz. In order to study the effect of input frequency on power and delay we change it from 50MHz to 500MHz.

The performance of the under test circuits were evaluated in term of worst-case propagation delay. Propagation delay was calculated from 50% of voltage level of input to 50% of voltage level of output. Rise time and fall time of input signals in the all simulations are 5% of the pulse width. In this study, power means the total average power consumption of the circuit, which calculated from equation (3).

$$vdd \int_0^{endsim} i_{vdd}(t)dt \qquad (3)$$

Where $i_{vdd}(t)$ is the instant current drawn from power supply and *endsim* is the duration time of simulation.

Power delay product has been calculated from production of worst-case delay and average power consumption according to equation (4).

$$PDP = Power_{average} \times Delay_{worst\text{-}case} \qquad (4)$$

Transistor sizing follows below rules. First $L=L_{min}=0.18\mu m$. Second, W for all NMOS transistors is equal to L_{min} and for PMOS Transistors is equal to $2L_{min}$. Third, if there are n serried transistors in a path the size of them become n times larger. Forth, the transistor sizes should be changed in order to optimize PDP in the circuit. In order to optimization worst-case delay and power should be studied.

All the circuits have been optimized in 1.8V supply voltage, 20fF output load and 200MHz input frequency conditions. To make fair comparison these conditions has been made same for all circuits as.

We use several input patterns to obtain average power consumption and worst-case delay in the under test circuits. Sample of the input pattern is shown in Fig. 13. In each pattern we tried to cover all possible cases of input values.

VII. Results and Discussion

A. *Output* waveforms

Fig. 13 shows the output waveforms for all the compared full adders.

As can be seen, outputs are not full swing. 10T, 9T and SERF have serious problem in output swing. Table II shows the worst values of voltage for logic 0 and logic 1. These values have been obtained from simulation.

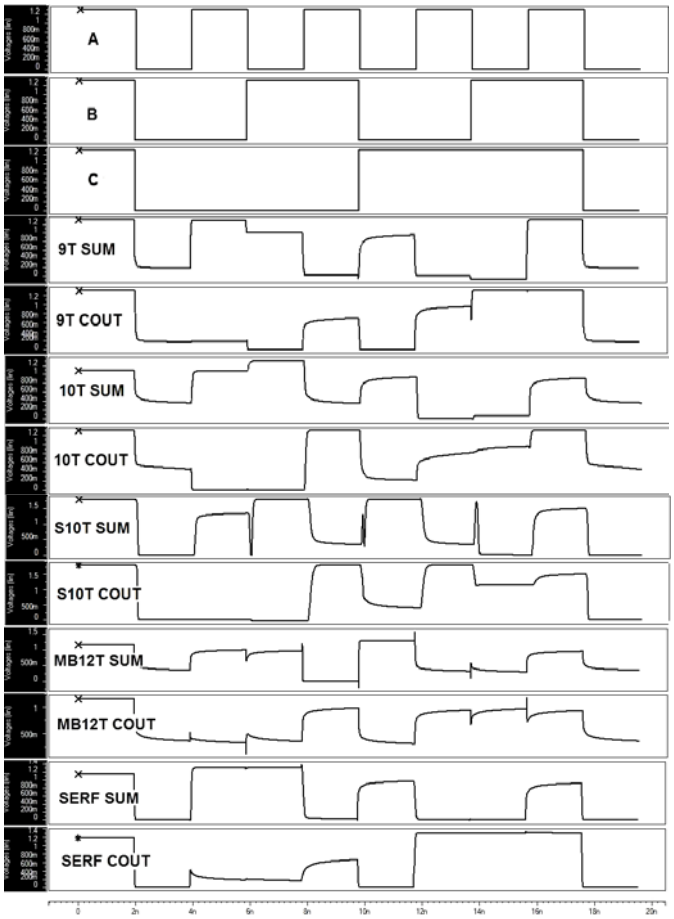


Fig. 13. Input and Output waveforms of simulated full adders.

Table II
Worst Output Voltage the Full Adders

Circuit	Min SUM Logic1	Max SUM Logic 0	Min COUT Logic 1	Max COUT Logic 0
SERF	1.4	0.04	1.15	0.32
MB12T	1.45	0.34	1.42	0.36
Prp. 9T	1.21	0.42	1.19	0.42
10T	1.41	0.31	1.26	0.31
Prp. S10T	1.16	0.36	1.15	0.35

B. *Power Comparison*

In this section, we study the effect of supply voltage variation vs. power, delay and PDP. We changed the supply power from 1.1V to 1.8V. 10T full adder is the most power

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consuming circuit. The power consumption gets worst with increasing the power supply.

S10T has less power consumption than the other circuits. It worked successfully in low voltage supply power. In term of power consumption, SERF positioned after MB12T. The 9T full adder consumes high power due to use of high power consumption XOR gate. However, that circuit consumes less power than 10T full adder. 10T use one three-transistor XNOR and one three-transistor XOR circuit. This is the reason of high power consumption in 10T circuit.

Output load is one of the important parameters that affects power and performance of the circuits. Here we changed output loads from 2fF to 500fF. S10T is the best circuit in term of power consumption for all values of output loads. The number of transistors in 9T is less than SERF and S10T but power consumption is higher than those circuits. The power of SERF changes sharply by increasing the output load value.

Input frequency was changed from 50MHz to 500MHz and the effect of that was studied.

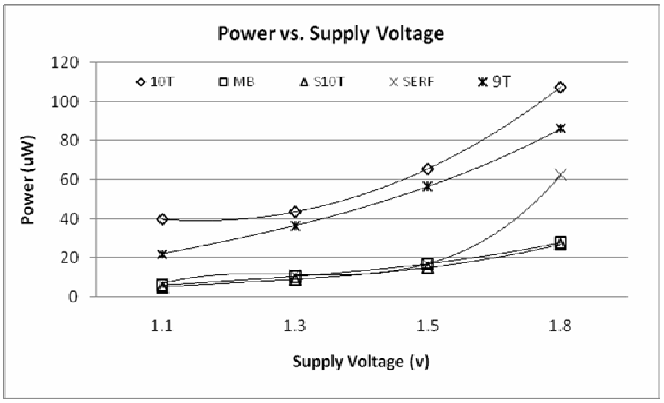
The results are in Fig. 14(c). This Figure shows that decreasing the frequency decreases the power consumption. S10T shows the best power consumption among all the other circuits in high frequency. In low frequencies, SERF is better than other circuits in term of power consumption. It shows that SERF circuit is a suitable full adder to use in low frequency and S10T is suitable to use in high frequency. The 9T full adder does not show good power consumption. Fig. 14(c) shows that 9T circuit has high sensitivity against frequency changing among all the circuits. The least power consumption circuit is the proposed full adder with the mixed 4T XNOR and the proposed logic approach.

C. Delay Comparison

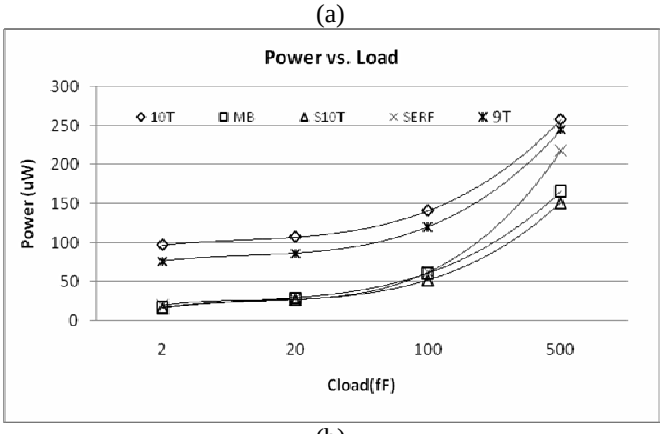
Similar to previous experiments, we changed the supply voltage, output load and input frequency in all circuits. They were studied in term of average propagation delay. As Fig 14. (d) shows SERF is the worst circuit in term of speed except in VDD=1.8V. It has high delay and high sensitivity against voltage scaling. The worst delay is to produce COUT signal. There are three serried transistors in the path of generation of the COUT. MB12T keeps a high distance from SERF and shows better performance than SERF shows. 9T and 10T have almost the same delay. In low voltage, 9T shows better delay than 10T. MB12T and S10T have almost same delay in low voltages. However, in 1.8V supply voltage S10T is faster than MB12T. High speed of the proposed full adders is due to short path between input and output. In the worst case, there is two serried transistors delay between input and output. Table III shows the values of the experiments for 1.8V, 200MHz and 20fF output load to show differences better.

Fig. 14(e) shows, the delay vs. output load. In high output load, 9T is the fastest circuit. S10T is in the second position after 9T in term of delay in high output load. S10T shows less delay than MB12T in all output loads.

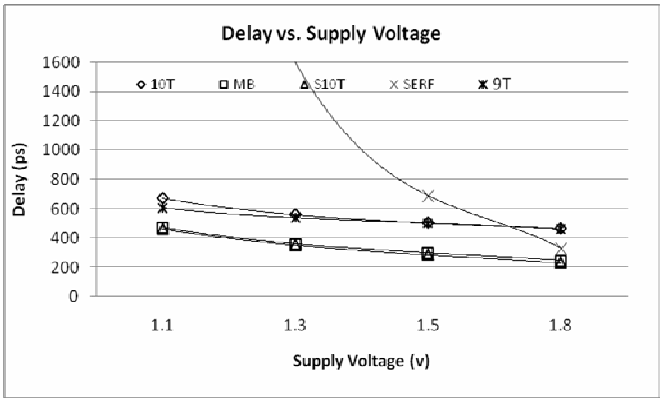
Fig. 14(f) shows, S10T has less delay in all frequencies in comparison to the other circuits. When input frequency is equal to 500MHz, 10T is faster than SERF and 9T. Glitches in producing intermediate signal simultaneously cause to high delay and power consumption in low frequencies in this circuit.



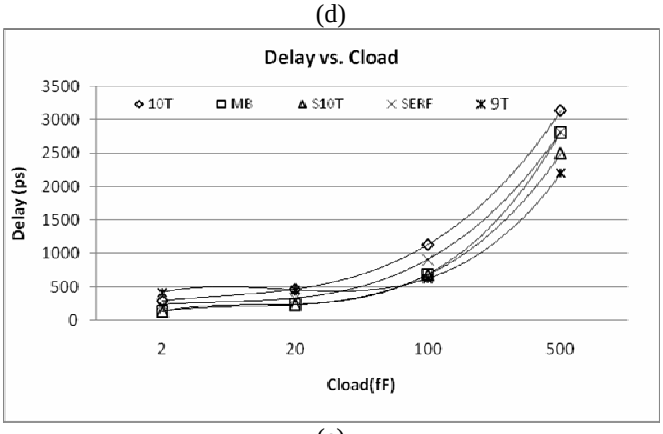
(a)



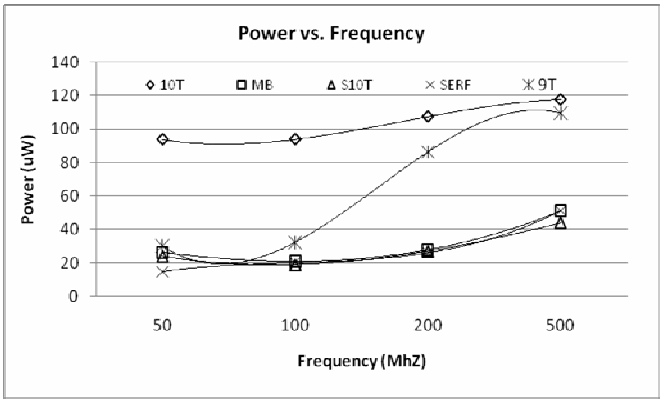
(b)



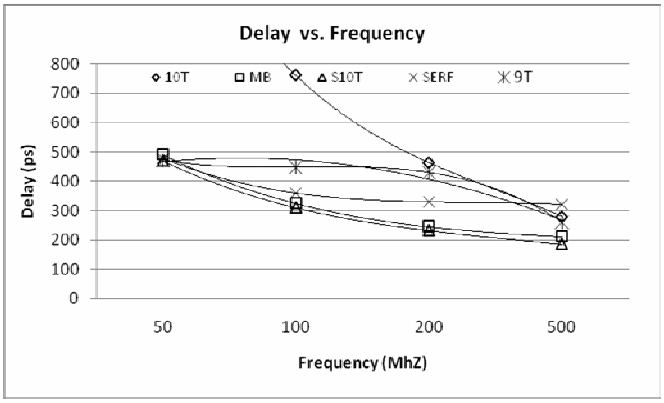
(d)



(e)



(c)



(f)

Fig. 14. Power and delay comparison vs. supply power, output load and frequency. (a) Power consumption vs. supply voltage. (b) Power consumption vs. output load (c) Power consumption vs. input frequency (d) Delay vs. supply voltage (e) Delay vs. output load (f) Delay vs. input

TABLE III
SIMULATION RESULTS FOR 1.8V, 20FF AND 200MHZ.

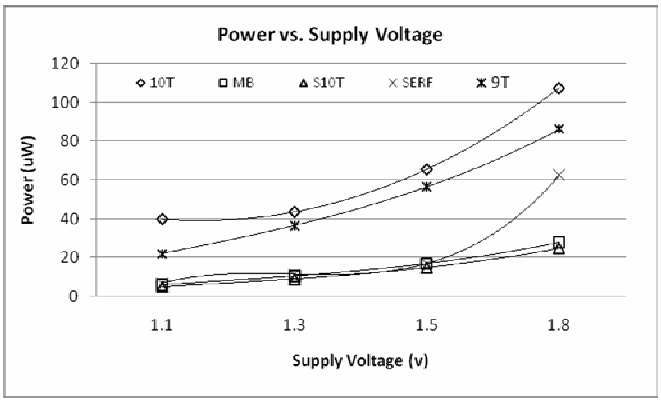
	Power (e-6)	Delay (e-12)	PDP(e-18)	No. Tr.
SERF	63	329	20	10
MB12T	28	245	6.9	12
Proposed 9T	86	461	39	9
10T	107	464	49	10
Prposed S10T	25	232	5.8	10

D. PDP Comparison

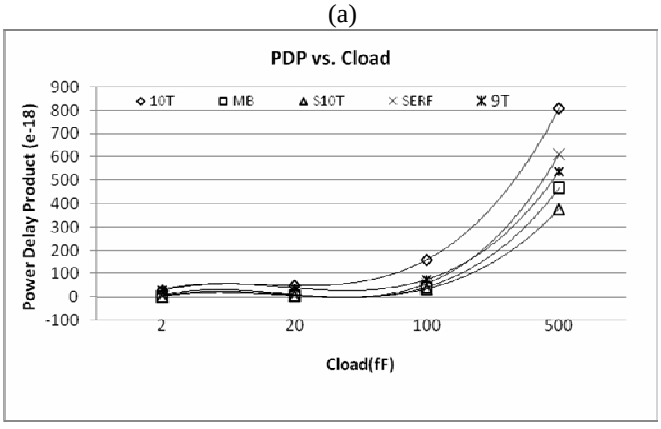
Fig. 15 shows the power delay product of the compared circuits. The conditions are same as power and delay experiments. The effect of supply voltage on PDP has been shown in Fig. 15(a). In low voltages, 9T is better than SERF and 10T. Fig. 15(a) shows S10T and MB12T have almost same PDP but Table II shows that there are improvements in power, delay and PDP in S10T design when we compare S10T to MB12T. Fig. 15(a) shows the best operating voltage for SERF in the condition of the experiment is 1.5V. All the time 9T has better PDP than 10T.

As shown in Fig. 15(b) S10T has lowest PDP in all output loads below 500fF. In case of 500fF output load, 9T has improvement in term of PDP in comparison to other circuits. In all output load values, MB12T is better than SERF is in term of PDP.

In low frequency, Fig. 15(c) shows SERF performs better than others do. However, in high frequency, S10T is the best circuit. MB12T has less PDP than SERF, 9T and 10T in frequencies above 50MHz. In low frequencies, it has higher PDP than SERF and S10T. 9T and 10T have almost the same PDP in 500MHz frequency.



(a)



(b)

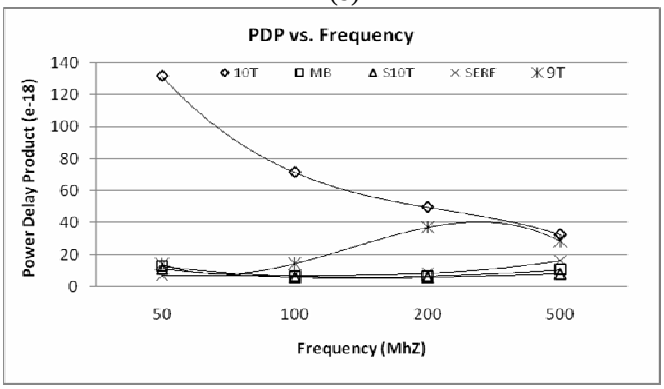


Fig. 15. (a) PDP vs. supply voltage. (b) PDP vs. output load. (c) PDP vs. input frequency

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TABLE IV
IMPROVEMENTS

	Power	Delay	PDP
SERF	0.44	0.74	0.29
MB12T	1	1	1
9T	0.32	0.53	0.17
10T	0.26	0.52	0.14
S10T	1.12	1.05	1.18

VIII. CONCLUSION

Two low power high performance 1-bit full adder cells were proposed in this paper. The new full adders were implemented using two alternative approaches that use only one XOR or XNOR gate. Both proposed full adders were tested in various conditions such as various output loads, supply voltages and input frequencies and they show good power consumption and performance. Two new full adders, SERF, MB12T and 10T were compared in terms of power, delay and PDP using HSPICE. The results showed that S10T is 12% faster than MB12T and the power is 5% times less than MB12T. 9T showed 24% improvement in term of power consumption in comparison to 10T in term of power.

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