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Digital Power Management Hardware Realization Using FPGA

Kar Foo Chong, Andreas Lee Astuti, Pradeep K. Gopalakrishnan and T. Hui Teo

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***Abstract*—**This paper describes design of a digital feedback loop for a low switching frequency dc-dc switching converters. Low switching frequencies were selected in this design. A look up table for the digital PID (proportional integrator differentiator) compensator was implemented using Altera Stratix II with built-in ADC (analog-to-digital converter) to achieve this hardware realization. Design guidelines are given for the PID compensator, high frequency DPWM (digital pulse width modulator) and moving average filter.

***Keywords*—**dc-dc converter, FPGA, PID, power management,.

I. Introduction

DIGITAL controllers can offer a number of advantages over analog controllers, including flexibility, lower sensitivity, and programmability without external component.

Fig. 1 shows the digital power management system.

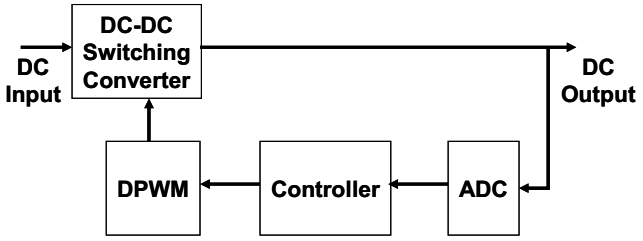

Fig. 1 Block diagram of a typical digital power management system

Fig. 1 delineates the basic building blocks of a dc-dc switching system. **Fig. 2** shows the circuit level implementation corresponding to this power management system.

In this design, the dc-dc converter is a closed loop circuit. The digital controller embedded within the FPGA (field programmable gate array) senses the output voltage through the Altera Stratix II board built-in ADC. The output voltage is then filtered using a moving average filter and compared to the reference voltage. The voltage difference results in an error signal. The PID compensator generates the corresponding duty cycle based on the error signal, [1]. The high frequency PWM generates control signal back to the analog circuit, which is the dc-dc switching converter to control the switching activity, [2].

This paper is organized as follows. Section II highlights the design specifications of the PID compensator, PWM and moving average filter. Design detail of the digital circuit and are given in Section III. Measured results are summarized in Section IV, with conclusion drawn in Section V.

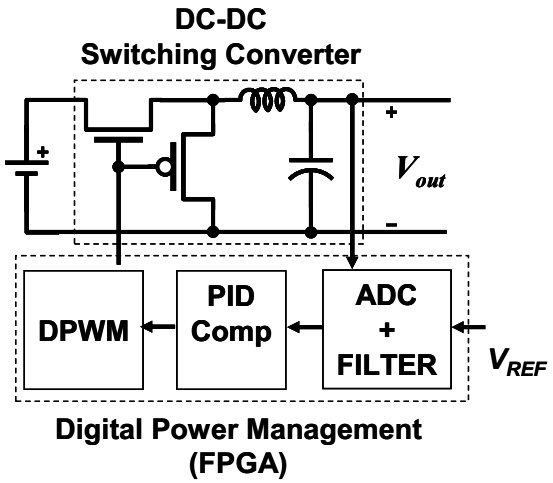

Fig. 2 Circuit implementation of the digital power management

II. Overall Design Specification

This featured decimator filter is targeting on operating at 3.3V ± 10% supply, across room temperature. The power consumption of the overall decimator filter is to keep below 300 μW. The switching frequency is 100 kHz. The total gate count should be below 15 k.

The design specifications of the buck converter are summarized in Table I.

TABLE I DESIGN SPECIFICATION OF THE BUCK CONVERTER

Parameter	Value	Units
Input Voltage	3.3	V
Output Voltage	1.8	V
Load	9 – 300	Ohm
Sampling Frequency	100k	Hz
Output Voltage Ripple	2%	

Based on the specifications in Table I, the inductance *L* and capacitance *C* are estimated as (1).

Kar Foo Chong, Andread Lee Astuti, Pradeep K. Gopalakrishnan and T. Hui Teo are with the Institute of Microelectronics, A*STAR (Agency for Science, Technology and Research), Singapore (phone: 65-67705323; fax: 65-67745754; e-mail: teehui@ime.a-star.edu.sg).

$$L = \frac{(1-D)\cdot R}{2\cdot f_{sw}} \qquad (1)$$
$$L = 680\mu H$$

with D: duty cycle, R: highest load value (taken to be 300 Ω), f_{sw}: switching frequency

In order to make sure the inductor current is continuous, the final inductance is estimated with (2).

$$L = 1.25\cdot 680 \qquad (2)$$
$$L = 850\mu H$$

In order to achieve voltage ripple 2%, the capacitance is estimated from (3),

$$C = \frac{1-D}{8\cdot L\cdot Ri\cdot f_{sw}^2} \qquad (3)$$
$$C = 0.33\mu F$$

with Ri is the output voltage ripple percentage.

The digital block design gate count and dynamic power were estimated using Synopsys DC (Design Compiler) tool. Table II summarizes the area and dynamic power estimation.

TABLE II GATE COUNT AND DYNAMIC POWER ESTIMATION OF VARIOUS DIGITAL BLOCKS IN BUCK CONVERTER

Block	Gate Count	Dynamic Power
DPWM	0.3 k	150 µW
ADC Decoder	11 k	9 µW
Compensator	0.8 k	6 µW
Overall	12.1 k	165 µW

III. CIRCUIT IMPLEMENTATION

If .

A. PID Compensator

The transfer function for the above switching power converter is as (4).

$$A(s) = \frac{V_{in}}{1 + s\frac{\omega}{Q} + s^2\frac{1}{\omega^2}} \qquad (4)$$

where V_{in} is the voltage supply, Q is the quality factor and ω is the natural frequency. The calculation of the Q and ω is as (5).

$$Q = R\cdot\sqrt{\frac{L}{C}} \qquad (5)$$
$$\omega = \frac{1}{\sqrt{L\cdot C}}$$

By referring to this transfer function of the plan, the PID compensator will be designed using Ziegler Nichols method.

Ziegle Nichols Design Method is summarized as the following steps.

1. Transfer the transfer function of the switching power converter from s-domain to z-domain by using ZOH method. Assume you will get *A(z)*.
2. Assume the PID compensator transfer function is as (6).

$$Gc(z) = K_P + K_D\cdot\frac{z-1}{T\cdot z} + K_I\cdot\frac{T\cdot z}{z-1} \qquad (6)$$

3. Initiate the procedure by multiple the *A(z)* with the above PID transfer function (6). Set $K_D = K_I = 0$, then gradually increase the K_P until the system goes unstable.
4. At this value $K_P = K_X$ and note the frequency at which the system goes from begin stable to being unstable, the frequency of the oscillation, ω_X.
5. Then in the PID compensator, set

$$K_P = 0.6\cdot K_X$$
$$K_I = K_P\cdot\frac{\omega_X}{\pi} \qquad (7)$$
$$K_D = K_P\cdot\frac{\pi}{4\cdot\omega_X}$$

6. Fine-tuning can be achieved by iterating on the K_I and K_D values, gradually decreasing K_I and increasing K_D.
7. The transfer function for the PID compensator is as (8).

$$B(z) = \frac{C_1\cdot z^2 + C_2\cdot z + C_3}{z^2 - z}$$
$$C_1 = K_P + K_I\cdot T + \frac{K_D}{T} \qquad (8)$$
$$C_2 = -\left(K_P + 2\cdot\frac{K_P}{T}\right)$$
$$C_3 = \frac{K_P}{T}$$

Fig. 3 below shows the result of the Ziegle Nichols design method for the PID compensator.

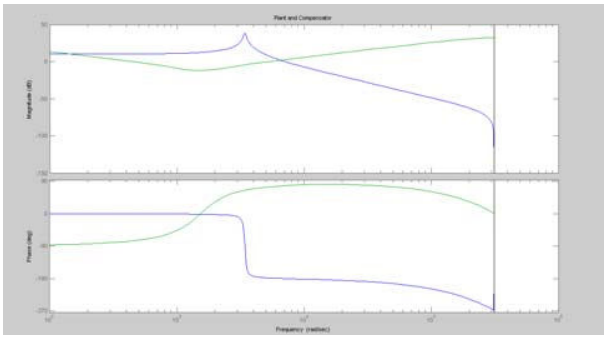

Fig. 3 Plant and compensator

Fig. 4 shows the frequency responses of the plan, compensator and the closed loop system.

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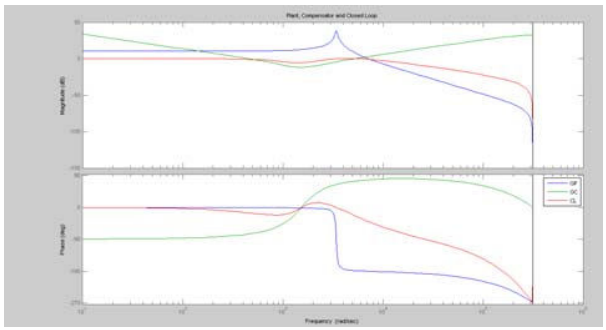

Fig. 4 Frequency responses of the plant, compensator, and overall closed loop system

Fig. 5 below shows the step response of the closed loop system.

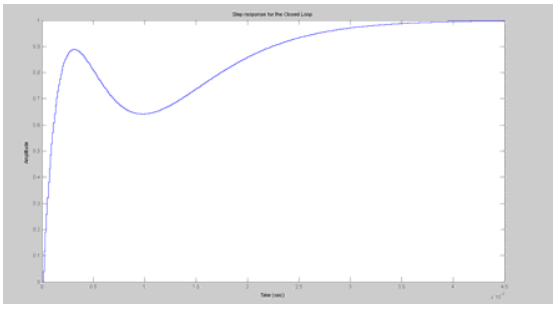

Fig. 5 Step response of the closed loop system

The PID compensator is the key design block in this buck converter. This block will translate the error signal from the ADC to the corresponding duty cycle to maintain the output voltage. The compensator block consists of three look up tables, which contain the pre-calculated multiplication results between the coefficient of the compensator and the error voltage. **Fig. 6** shows the block diagram of the PID compensator circuit.

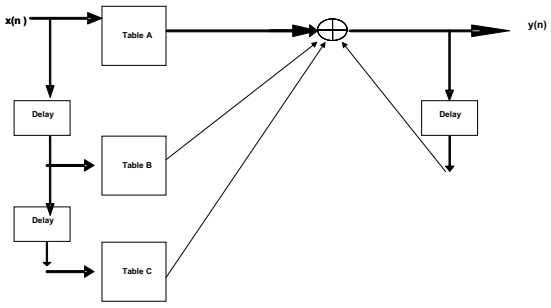

Fig. 6 PID compensator

B. ADC And Moving Average Filter

In this design, the built in ADC of the Altera Stratix II board was used for the digital buck converter design. The required specifications are summarized as follow.

Max output voltage = 1.8V + 160mV = 1.96V

V_{REF}= 91.8% of the A/D full range voltage

ADC_{RES}= 40mV (2.2% variation)

ADC_{Gain} = 1/40mV = 25

Number of ADC output bit = 7 bit > $\text{int}\left(\log_2\left(\frac{1}{ADC_{RES}\cdot V_{REF}}\right)\right)$

Because FPGA ADC is sensitive to the minor change in the output voltage of the switching power converter circuit, a 64 stage moving average filter was implemented to filter out the noise. **Fig. 7** shows the input and output signals of the moving average filter.

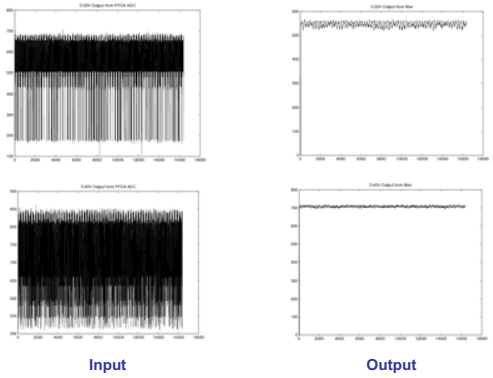

Fig. 7 Input and output signals of the 64 stages moving average filter

C. DPWM

PWM architecture used in this design is the high frequency modulator, [3]. PWM block generates pulse waveform back to the switching converter circuit. There is a 8-bit counter inside the PWM block. PWM block generates number of logic '1' equivalent to the counter value. The rest of the value will be output as logic '0'. The total number of bit for PWM, N_{DPWM} is estimated from (9).

$$N_{DPWM} = N_{ADC} + 1$$
$$f_{CLK} = 2^N \cdot f_{SW} \quad (9)$$

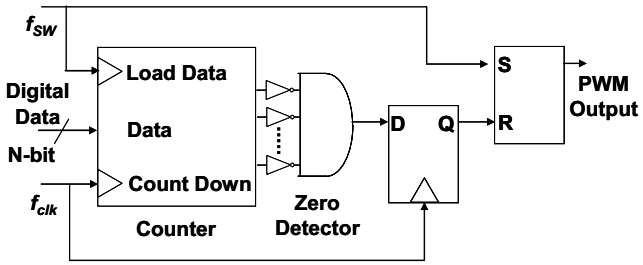

Fig. 8 DPWM circuit implementation

IV. Hardware And Measurement

A simple prototype was built to demonstrate the design. **Fig. 9** shows the prototype of the buck converter system.

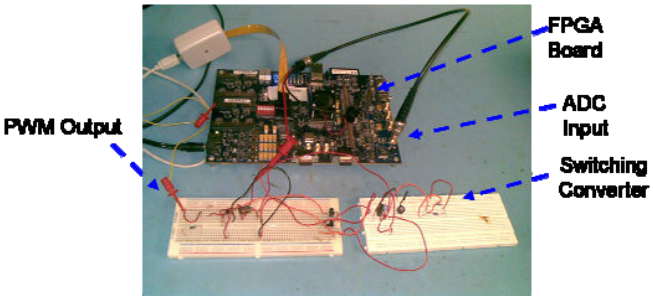

Fig. 9 Digital assist buck converter prototype

The output of the switching power converter measured using oscilloscope. **Fig. 10** shows the steady state voltage waveform. This shows the functionality of the bulk converter using digital PID compensator.

Fig. 10 Snapshot of the bulk converter output voltage

V. Conclusion

In this paper we describe the design and implementation of the digital power management prototype which results in a fast and simple hardware realization with FPGA. Design guidelines for the hardware implementation were given and demonstrated on an example of a digitally controlled buck converter operating at 100 kHz switching frequency.

Acknowledgment

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