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Analytical Modeling of Channel Noise for Gate Material Engineered Surrounded/Cylindrical Gate (SGT/CGT) MOSFET

Pujarini Ghosh A, Rishu Chaujar B, Subhasis Haldar C, R.S Gupta D and Mridula Gupta E

Abstract**—**In this paper, an analytical modeling is presentated to describe the channel noise in GME SGT/CGT MOSFET, based on explicit functions of MOSFETs geometry and biasing conditions for all channel length down to deep submicron and is verified with the experimental data. Results shows the impact of various parameters such as gate bias, drain bias, channel length ,device diameter and gate material work function difference on drain current noise spectral density of the device reflecting its applicability for circuit design applications.

Keywords**—**Cylindrical/Surrounded gate (SGT/CGT) MOSFET, Gate Material Engineering (GME), Spectral Noise and short channel effect (SCE).

I. Introduction

OVER the past few years, reduction in channel length which leads to short-channel effects (SCEs)[1] such as threshold voltage (Vth) roll-off and drain induced barrier lowering (DIBL) are becoming increasingly important in integrating deep submicron CMOS devices. It degrades the device performance as the gate voltage control over the drain current is reduce due to increase in charge sharing from the drain/source region.

In order to overcome the scaling limitations on planar devices and to achieve high packing density for future circuit designing, the Cylindrical/ surrounded gate MOSFET (CGT/SGT) MOSFET[2] is one of the promising solutions for controlling SCEs as well as improving subthreshold slope, high current drive and packing densities.

In the past few years, various studies had been carried out on CGT/ SGT MOSFETs [5][6][7] to reduce the short channel effect. M.J Kumar et.al, [3] on the other hand, studied Vertical MOSFETs by applying gate material engineering, in which dual material gate architecture has been incorporated to reduce the SCEs and improve the carrier transport efficiency. To integrate the advantages of GME and CGT/SGT, a new structure has been proposed, named as GME SGT/CGT MOSFET. (Fig. 1)

In addition to the high levels of integration for digital circuit design which is offered by CMOS processes, the SGT/CGT MOSFETs are also capable of operating in the GHz regime because of their very high unity-gain frequencies of tens of GHz. As a result, MOSFETs have become very attractive for RF IC applications [4]. The noise generated within the device plays an increasingly important role while operating at higher frequencies, in the RF IC applications; e.g., in the noise performance of a front-end receiver in an RF IC.

Therefore a physics based analytical channel noise model which can accurately predict the noise characteristics of deep submicron MOSFETs is crucial for the low noise RF IC designing.

II. Analytical Channel Noise

The channel noise expression is obtained by dividing the channel region into two parts: linear region and saturation region. It is assumed that most of the drain current noise of MOSFET is generated in the linear region, and is negligible in velocity saturation region. This is due to the fact that the carriers travel at their saturation velocity and therefore, they do not respond to the electric field fluctuations caused by the voltage fluctuation in the channel [8]. The MOSFETs drain current in strong inversion is dominated by the drift current and can be expressed at any point z in the channel as

$$I = -\pi R Q(z) v(z) \tag{1}$$

Where π.R is the width of the device and R is the diameter of the device, $Q(z)$ is charge per unit area and $v(z)$ is the velocity of the carriers along the channel. According to the BSIM model [9], the channel charge per unit area can be expressed as a function along the channel length

$$Q(z) = -C_{ox}(V_{gt} - \alpha V(z)) \tag{2}$$

Where C_{ox} is gate capacitance per unit area.

$V_{gt} = V_{th} - V_{gs}$ and V_{th} is the threshold voltage, α is the bulk-charge effect coefficient and taken as (α =1.2) [9] and V(z) is the potential that varies along the channel from 0 at the

Author A,E is with the Semiconductor oratory, Department of Electronic Sciences, University of Delhi, South Campus, New Delhi (India) -110021. (corresponding author phone:91-11-24115580;fax:91-11-24110606; e-mail: mridula@south.du.ac.in, puja510@gmail.com).

Author B, is with the Department of Electronics, Deen Dayal Upadhyaya College, Karampura, University of Delhi, New Delhi-110015.

Author C is with the Department of Physics, Motilal Nehru College, University of Delhi, New Delhi (India)- 110021.

Author D, is with the Department of Electronic & Communication Engineering, Maharaja Agrasen Institute of Technology, Sector -22, Rohini, Delhi (India) -110085; e-mail: rsgu@bol.net.inDevice Research Lab

source side to the V_{DS} at the drain side. The carrier velocity is given by a piecewise model [11] as

$$v(z) = \begin{cases} \dfrac{\mu_{eff} E(z)}{1+\dfrac{E(z)}{Ec}} \rightarrow E(z) \langle E_c \\ v_{sat} \rightarrow E(z) \rangle E_c \end{cases} \quad (3)$$

Where $E(z)$ electric field along the channel in z direction, $E(c)$ critical electric field and is equal $\frac{2v_{sat}}{\mu_{eff}}$, v_{sat} is the saturation velocity and μ_{eff} is effective mobility of the carriers. Substituting (2) and (3) in (1), one obtains the current in the linear regions of the channel as,

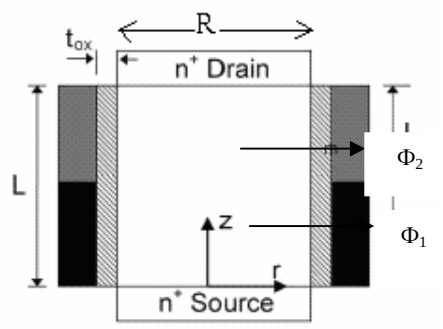

Fig.1. Cross sectional view of the GME SGT/CGT MOSFET. $t_{ox=}$ 100 Å, πR=60μm, L=180nm, Φ_1=4.8eV, Φ_2=4.4eV, $N_D = 10^{12}$, V_{gs}=1V and V_{ds}=1.5V Unless stated otherwise.

$$I_{dL} = \mu_{eff} W C_{ox} (V_{gt} - \alpha V(z) \frac{\dfrac{dV(z)}{dz}}{1+\dfrac{dV(z)}{E_c dz}} \quad (4)$$

Where $E(z) = \dfrac{dV(z)}{dz}$ and (5)

$V(z)$ is the channel potential along the z direction.

To calculate the drain current noise, the linear part of the channel is taken under consideration as the channel noise is negligible in the velocity saturation region. Thus the drain current spectral noise is given as[10]

$$S_{idL} = 4kT \frac{4V^2_{gt} + V_0^2 - 2V_0 V_{gt}}{3V^2_{gt}(V_{gt} - V_0)} \alpha I \quad (6)$$

From equation (4), it is seen that at the point along the channel where the carrier velocity is saturated i.e. $v(z) = v_{sat}$, then the drain current becomes

$$I_{dsat} = WC_{ox}(V_{gt} - V_{Dsat}\alpha) v_{sat}$$

where

$$V_0 = V_{gt} - \alpha V_{Dsat} ,$$

Consequently, equation (6) becomes

$$S_{idsat} = 4kTI \left[\frac{1}{V_{Dsat}} + \frac{\alpha^2 V_{Dsat}}{3V_{gt}^2} \right] \quad (7)$$

This is the equation for drain current noise spectral density of the device in the saturation region. The net drain current spectral noise density is the summation of the drain current spectral noise in both the region that is linear and the saturation.

III Results and Discussions

In this section we have analyzed our modeled result of drain current noise spectral density of GME SGT/CGT MOSFET as a function of gate bias, drain bias, channel length, diameter and work function.

Fig.2 shows the variation of drain current noise spectral density with respect to gate to source voltage with drain voltage constant at 1.5V. From the figure, it is observed that, with the increase in gate bias the drain current noise spectral density decreases in the GME SGT/CGT MOSFET. The overall noise in case of GME MOSFET is much less as compare to the convention MOSFET. Further, if we reduce the channel length from 180nm to 100nm the drain current noise spectral density also reduces due to improve in gate control and better screening of channel region as metal gate work function in GME SGT/CGT MOSFET is different as compare to conventional MOSFET.

Fig.3: Shows the variation of drain current noise spectral density with respect to drain voltage for V_{gs} = 1V. From the figure, it is observed that the drain to current noise spectral density remains constant throughout the drain bias as in a short channel device , the thermal noise attains a constant value after a certain drain current (optimal current)[5]. Again overall drain current noise is lesser as compare to the conventional MOSFET and also decreases as channel length reduces from 180nm to100nm.

Fig. 4: shows the variation of the drain current noise spectral density with respect to different work function of the metal near the drain. In the figure, it is observed that as the gate bias increases the drain current noise spectral density decreases for a constant work function due to the fact that the drain current noise spectral density is inversely proportional to

the gate to source voltage (7). With the increase in work function of the gate metal near the drain the spectral noise increases. This is because the increased metal work function at the drain end approaches that of the source end thereby making the work function of the entire gate region nearly uniform. Thus the peak electric field in the channel is now produced near the drain end. Hence efficiency reduces and noise increases.

Fig. 5: shows the variation of the drain current noise spectral density with respect to the diameter of the GME SGT/CGT MOSFET using two different gate biases at 1V and 1.5V.

Fig. 6: shows the variation of the drain current noise spectral density with respect to the channel length of the GME SGT/CGT MOSFET using two different gate biases voltages i.e. V_{gs}=1V and V_{gs}=1.5V. In both the above figures, it has been observed that as the gate bias increases, the drain current noise spectral density reduces.

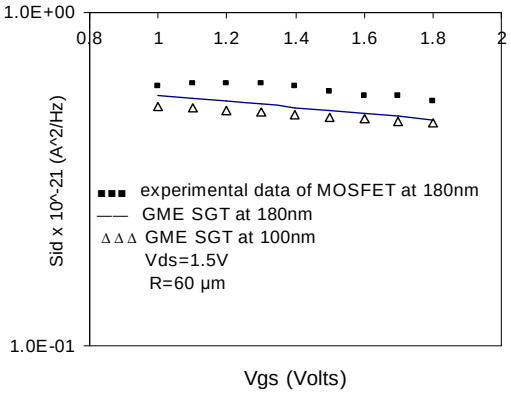

Fig. 2. Channel thermal noise of GME SGT MOSFET versus Vgs at channel length of 180nm and is compared with the experimental data.

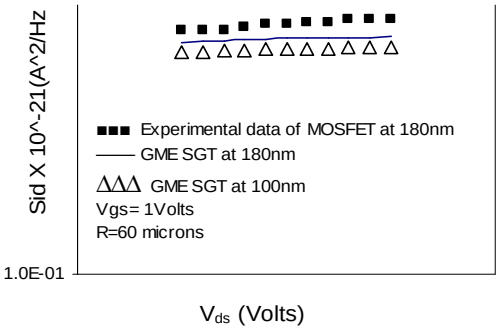

Fig. 3. Channel thermal noise of GME SGT MOSFET versus Vds at channel length of 180nm and is compared with the experimental data.

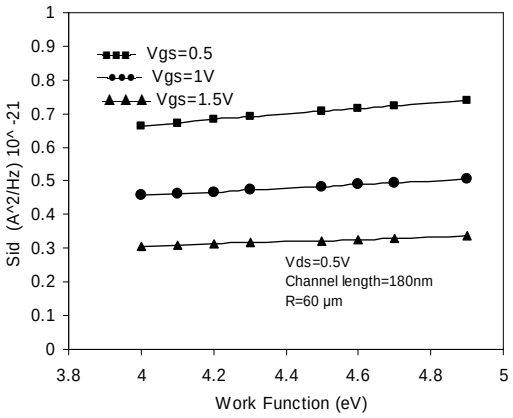

Fig. 4. Channel thermal noise of GME SGT MOSFET versus gate material work function difference.

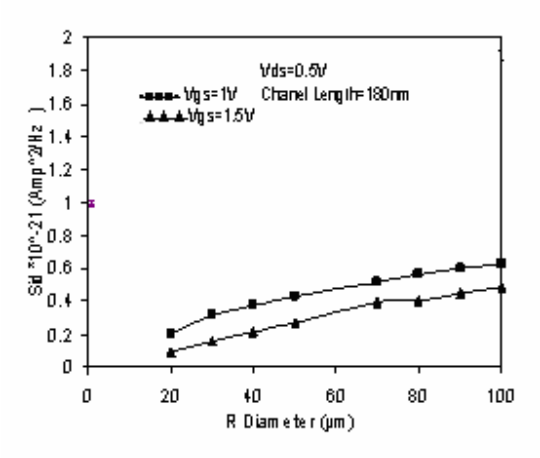

Fig. 5. Channel thermal noise of GME SGT MOSFET versus different device diameter.

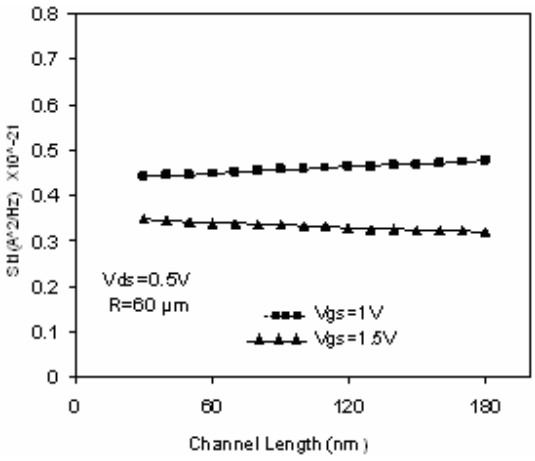

Fig. 6. Channel thermal noise of GME SGT MOSFET versus different channel length.

IV Conclusion

Analytical modeling of the GME SGT/CGT MOSFETs channel noise was presented and verified with experimental data of conventional MOSFET. The expression of channel noise were explicit functions of MOSFET geometry and biasing conditions, and hence can be used for circuit designing purposes.

Moreover, it was demonstrated that as the channel length of the device decreases the effect of noise spectral density also reduces as well as , as the gate voltage increases the channel noise also decreases. Thus it is concluded that GME SGT/CGT MOSFET structure reduces short channel effect.

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