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Uniform Overlapped Multi-Carrier PWM for a Six-Level Diode Clamped Inverter

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***Abstract*—**Multi-level voltage source inverters offer several advantages such as; derivation of a refined output voltage with reduced total harmonic distortion (THD), reduction of voltage ratings of the power semiconductor switching devices and also the reduced electro-magnetic-interference problems etc. In this paper, new carrier-overlapped phase-disposition or sub-harmonic sinusoidal pulse width modulation (CO-PD-SPWM) and also the carrier-overlapped phase-disposition space vector modulation (CO-PD-SVPWM) schemes for a six-level diode-clamped inverter topology are proposed. The principle of the proposed PWM schemes is similar to the conventional PD-PWM with a little deviation from it in the sense that the triangular carriers are all overlapped. The overlapping of the triangular carriers on one hand results in an increased number of switchings, on the other hand this facilitates an improved spectral performance of the output voltage. It is demonstrated through simulation studies that the six-level diode-clamped inverter with the use of CO-PD-SPWM and CO-PD-SVPWM proposed in this paper is capable of generating multiple levels in its output voltage. The advantages of the proposed PWM schemes can be derived to benefit, especially at lower modulation indices of the inverter and hence this aspect of the proposed PWM schemes can be well exploited in high power applications requiring low speeds of operation of the drive.

***Keywords*—**Diode clamped inverter, Pulse width modulation, Six level inverter, carrier based PWM.

I. Introduction

RESEARCH on various multi-level inverter power circuit topologies has extensively increased ever since the neutral-point-clamped three-level inverter configuration was first introduced by Nabae et.al. [1]. The multi-level inverters offer several advantages such as, less stresses on the switching devices, less THD in the output of the inverters, less ripple in the output voltage and a better spectral performance of the inverters etc. It was demonstrated that, refined output voltage can be obtained either by using smaller imbricated cells or the cascaded inverter structures [2]-[6]. H.Stemmler and P.Guggenbach through their research synthesized three-level output by using series cascading of two two-level inverters using induction motor with open-end stator windings [5]. Recently, it was established that using cascaded retrofit of two two-level inverters, three-level output voltage can also be synthesized [6]. While each of the proposed circuits has some drawbacks, they have their own merits as compared to the others. These circuits are slowly being accepted by the industry in the recent times and are the focus of many researchers now.

Several multilevel PWM switching schemes have been proposed in the past and an extensive survey of PWM schemes has also been reported in the literature [7]. Improved spectral performance and enhanced DC-bus utilization is also achieved by altogether modifying the sinusoidal modulating signal by either adding appropriate third harmonic component or giving suitable offset voltages [7]-[9]. Triangular multi-carriers are uniformly distributed with their phases adjusted to suit the application is reported in the past [10]-[13]. Multilevel PWM with modified triangular carriers are also reported in the literature for a multi-level inverter [14]-[15].

In this paper, uniform, zero phase shifted, overlapped multi-carrier PWM switching schemes are proposed using the conventional SPWM and also the SVPWM for a six-level diode-clamped inverter circuit topology. It is eloquently demonstrated through simulation studies that the spectral performance of the output voltage using the overlapped carrier PWM proposed in this paper is improved as compared to the use of the conventional PD-PWM especially in the lower modulation range. The main drawback with the use of the proposed PWM is the increased total number of switchings; resulting in an increased switching power loss. However, the improved spectrum of the output voltage with the proposed PWM scheme could offset the increased switching power loss.

II. Diode-clamped six-level inverter

The schematic of the three-phase six-level diode-clamped inverter configuration is shown in Fig.1. Each of the three phases of the inverter, share a common DC-bus, which has been subdivided into six levels, using five capacitors. The voltage across each capacitor is equal to a voltage of $V_{DC}/5$, and the voltage stress across each switching device is therefore limited to $V_{DC}/5$ through the clamping diodes. The output voltage levels possible for one phase of the inverter (Fig.1) with the negative dc rail voltage 'V_0' (equal to zero volts), taken as the reference are tabulated and presented in Table-I. In Table-I, a 'P' means, the switch is turned ON and an 'N' means, the switch is turned OFF. In Fig.1, each phase has five complementary switch pairs such that turning-on one of the switches of the pair require that the corresponding

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complementary switch be turned off and vise-versa. The complementary switch pairs for a-phase limb are (SW_{a1}, $SW_{a1'}$), (SW_{a2}, $SW_{a2'}$), (SW_{a3}, $SW_{a3'}$), (SW_{a4}, $SW_{a4'}$), and (SW_{a5}, $SW_{a5'}$). Table-I, also shows that in a diode-clamped inverter, the switches that are turned on for a particular phase limb are always adjacent and in series. It is known that in a six-level diode-clamped inverter topology, a set of five switches are turned on at any given point of time.

The line voltage V_{AB} consists of a-phase limb voltage and b-phase limb voltage. The resulting line voltage is an eleven level staircase waveform [11]. This means that an m-level diode-clamped inverter has an m-level output phase voltage and a (2m-1)-level output line voltage [11]. Although each active switching device is required to block only a voltage level of $V_{DC}/5$, the clamping diodes require different ratings for reverse voltage blocking. In phase 'a' (Fig.1), when all the lower switches $SW_{a1'}$ through $SW_{a5'}$ are turned-on, D_4 must block four voltage levels or $4V_{DC}/5$. Similarly, D_3 must block $3V_{DC}/5$, D_2 must block $2V_{DC}/5$ and D_1 must block $V_{DC}/5$. If the inverter is designed such that each blocking diode has the same voltage rating as the active switches, D_n will require 'n' diodes in series; consequently, the number of diodes required for each phase would be (m-1) × (m-2). Thus, the number of blocking diodes is quadratically related to the number of levels in a diode-clamped converter [11].

III. Multilevel carrier-based PWM

Principles of several two-level carrier-based PWM techniques have been extended as means of controlling the active devices in a multilevel converter. The most popular control technique for traditional two-level inverters is the sinusoidal or "sub-harmonic" natural pulse width modulation method which uses several triangle carrier signals and one reference or modulation signal per phase. Its popularity is due to its simplicity and the good results it guarantees in all the operating conditions, including over-modulation which allows first harmonic amplitude up to (4 /Π) p.u. In order to achieve enhanced DC-bus utilization and also improved spectral performance, the modified reference signal is adopted, using sinusoidal fundamental along with third harmonic injection of an appropriate magnitude or with appropriate offset voltages.

The three multilevel PWM methods most discussed in the literature for the multi-level inverters have been multilevel carrier-based PWM, selective harmonic elimination, and multilevel space vector PWM; all are extensions of traditional two-level PWM strategies to several levels. Several variations

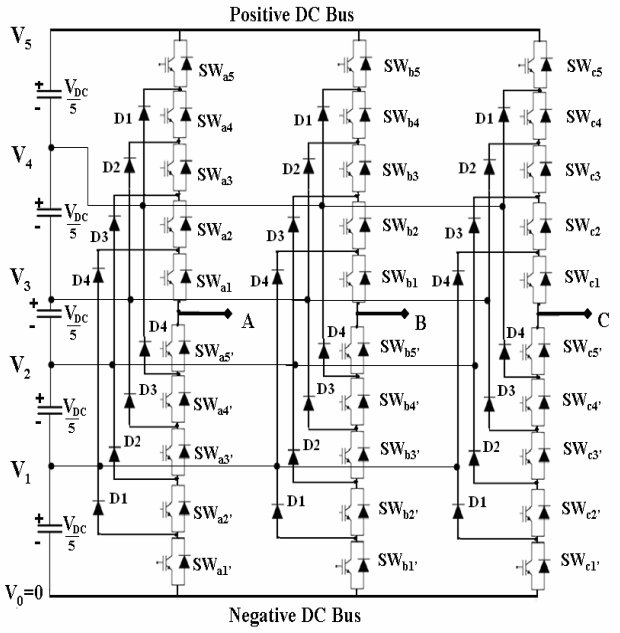


Fig. 1 Schematic of the six-level diode-clamped inverter configuration

TABLE- I SIX-LEVEL DIODE-CLAMPED INVERTER VOLTAGE LEVELS AND CORRESPONDING SWITCH STATES

Voltage V_{AO}	$V_5=V_{DC}$	$V_4=\frac{4V_{DC}}{5}$	$V_3=\frac{3V_{DC}}{5}$	$V_2=\frac{2V_{DC}}{5}$	$V_1=\frac{V_{DC}}{5}$	$V_{0=}$ **0**
SW_{a5}	P	N	N	N	N	N
SW_{a4}	P	P	N	N	N	N
SW_{a3}	P	P	P	N	N	N
SW_{a2}	P	P	P	P	N	N
SW_{a1}	P	P	P	P	P	N
$SW_{a5'}$	N	P	P	P	P	P
$SW_{a4'}$	N	N	P	P	P	P
$SW_{a3'}$	N	N	N	P	P	P
$SW_{a2'}$	N	N	N	N	P	P
$SW_{a1'}$	N	N	N	N	N	P

of carrier-based PWM techniques adopting SPWM are applied to a multilevel inverter and are reported in the literature as phase opposition (PO), alternate phase opposition disposition (APOD) and sub-harmonic or phase disposition (PD) [10]-[11].

It is known that in the case of a conventional two-level inverter, each leg of the inverter can attain *two* voltage levels depending on whether the top switching device is turned on or the bottom switching device. Hence, the two-level three phase inverter has a total of 2^3 i.e. eight switching combinations; spread around 7 space locations; forming a regular hexagon shown in Fig.2 (each side equal to the DC-bus voltage 'V_{DC}' of the two-level inverter). In the case of the six-level diode-clamped inverter (Fig.1), each phase pole voltage (for instance V_{AO} shown in Table-I) can attain six levels independent of the other. Therefore, a total of 6^3 i.e. 216 switching combinations are possible that are spread

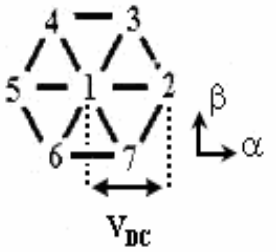


Fig. 2 Space locations of the conventional two-level inverter

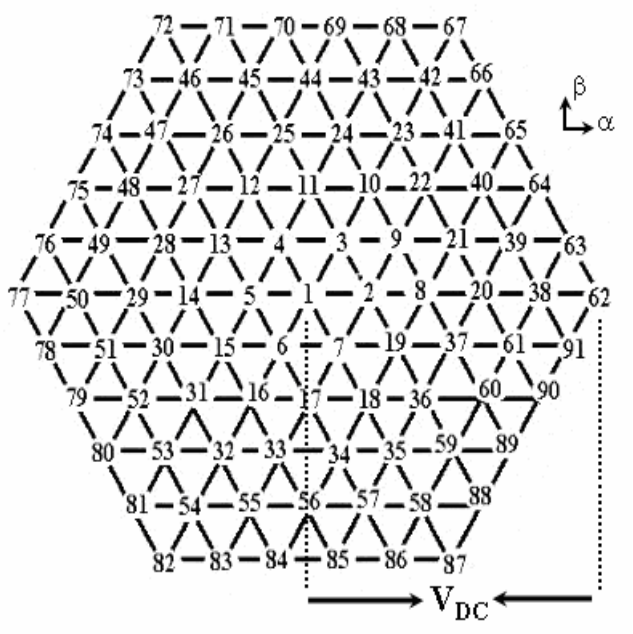


Fig. 3 Space vector locations of the six-level diode-clamped inverter

around 91 space locations shown in Fig.3. For instance, the switching combination (5,5,0) means that the a-phase and b-phase pole-voltage output is equal to V_{DC} each and the c-phase pole-voltage output is 0 volts. Substituting these conditions in the expression for the space vector, given by equation (1) and simplifying; results in the space location number 67 (Fig.3). The locations for the remaining switching combinations can be similarly obtained.

$$V_S = v_{AO} + v_{BO} \times e^{j(2\pi/3)} + v_{CO} \times e^{j(4\pi/3)} \quad (1)$$

For the six-level PWM method, triangular carrier signals keeping only one modulating sinusoidal signal is taken. Conventionally, it is well known that if an N-level inverter is employed, (N–1) carriers will be needed [10]. The carriers have the same frequency 'ω_c', and the same peak-to-peak amplitude A, are disposed so that the bands they occupy are contiguous. The modulating signal is a sinusoid of frequency 'ω_m', and amplitude A_m. At every instant each carrier signal is compared with the modulating signal. Each comparison gives two logic outputs depending on the instantaneous magnitudes of the modulating sinusoid and the carrier signal.

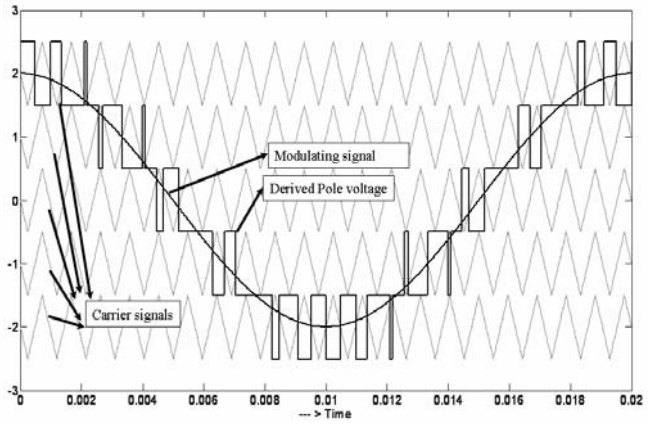


Fig. 4 Principle of the PD-SPWM and the derived pole voltage replica with the use of PD-SPWM

It gives an output of '+1' if the modulating signal is greater than the triangular carrier and an output of '0' when the modulating signal is lesser than the triangular carrier. It is generally accepted that with the use of PD-PWM strategy, the THD in the output voltage is less as compared to the CO-PWM and APOD-PWM [10]. The principle of the conventional PD-SPWM along with the resulting pole-voltage replica for a single phase is shown in Fig.4. Now, to comply with the requirements for a three-phase system, three 120^0 phase-shifted modulating sinusoids are compared with the level shifted triangular carrier set under single-phase modulation technique.

IV. Carrier-overlapped Sub-harmonic or phase diposition PWM for a Six-Level diode-claped Inverter

In the context of the present six-level diode-clamped inverter (Fig.1), the six-level carrier PWM is presented using the over-lapped, level-shifted, uniform zero phase-shifted, triangular carrier signals. Everything else remains the same, as in the conventional PD-SPWM, but for the overlapped triangular carrier signals. The principle of the proposed carrier-overlapped phase-disposition SPWM (CO-PD-SPWM) along with the derived pole voltage replica for a single phase of the six-level inverter is shown in Fig.5. From Fig.5, it may be seen that the total number of switchings in the phase is increased (doubled) as compared to the number of switchings shown in Fig.4 (using the conventional PD-SPWM) for the same frequency and amplitude modulation.

The principal advantage with the proposed CO-PD-SPWM is that the spectral performance of the output voltage is considerably improved. It is indisputable that increasing the switching frequency would alienate the lower order harmonics and improve the spectral performance of the output voltage.

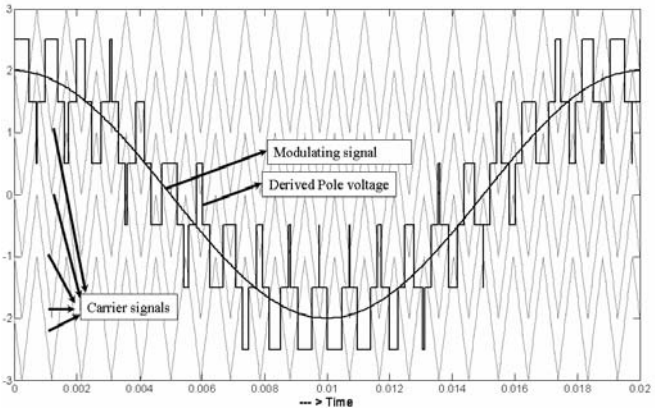


Fig. 5 Principle of the proposed CO-PD-SPWM approach and the derived pole voltage replica with the proposed CO-PD-SPWM

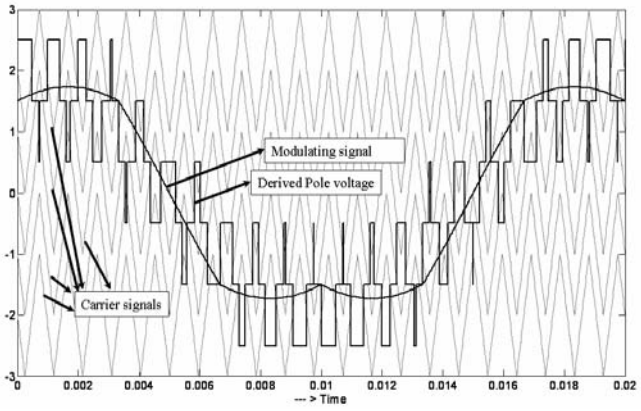


Fig. 6 CO-PD-SVPWM approach and the derived pole voltage replica with the proposed CO-PD-SVPWM

In order to draw attention onto the significance of the proposed PWM scheme and for proper comparison, the phase voltage is obtained using the proposed CO-PD-SPWM and also with the conventional PD-SPWM with doubled switching frequency. The normalized harmonic spectra of the phase voltage with the double switching frequency using conventional PD-SPWM is compared with the results obtained using the proposed CO-PD-SPWM and are shown in the later section.

As it is known that the use of the SVPWM would improve the DC-bus utilization, suitable offsets are added to the sinusoidal modulating signal and the over-lapped triangular carrier based implementation of SVPWM is also demonstrated. The CO-PD-SVPWM principle and the derived pole voltage replica of a single phase are shown in Fig.6.

It may be noted that while explaining the principle of operation using the schematics (Figs.4, 5, & 6) the modulating signal is chosen to be of 50Hz. However, in the actual simulation studies shown in the results, a constant V/f control is adopted in the linear modulation zone.

V. Results & discussions

The uniform, zero phase shifted, carrier-overlapped phase disposition or sub-harmonic carrier-based PWM for the multi-level inverter (six-level diode-clamped configuration) proposed in this paper are simulated using the MATLAB simulation software. The inverter is assumed to feed an induction motor load controlled with V/f control in the entire region of linear modulation and with constant terminal voltage (flux weakening operation) in the over-modulation region. Irrespective of the modulation depth, the frequency of the triangular carrier signal is chosen to be 21 times the fundamental frequency which means that there will be a total of 21 carrier cycles in one entire cycle of the fundamental. It is known that the length of the maximum voltage vector at the verge of linear-modulation is equal to $\sqrt{3}V_{DC}/2$ (radius of the largest circle inscribed in the hexagon shown in Fig.2). Hence, the frequency of the modulating signal is set equal to 50 Hz with the DC-bus voltage for the six-level inverter taken as 100Volts at the modulation depth 'm_a' equal to $\sqrt{3}/2$ i.e. 0.866 . The modulation depth 'm_a' is defined as the ratio of the magnitude of the space vector and the DC-bus voltage of the inverter. The motor would run at its rated speed corresponding to the fundamental frequency ('f_1') of 50Hz at this modulation depth.

A low speed of operation is obtained when the frequency of the modulating signal 'f_1' is set low. Corresponding to the fundamental frequency f_1=20Hz, the switching frequency of the inverter would be 420Hz and the modulation depth of the inverter would then be equal to 0.3464.

The a-phase pole voltage and its normalized harmonic spectrum, phase voltage (a-phase) and its normalized harmonic spectrum all taken when the fundamental frequency is equal to 20Hz are shown in Fig.7. It can be seen from the normalized harmonic spectra of the a-phase pole voltage (Fig.7.b) that the burst of harmonics are spread at and around the multiples of the frequency modulation i.e.21. Similarly, the results when the fundamental frequency is equal to 40Hz and 50Hz corresponding to two different motor speeds are respectively shown in Fig.8 & 9. From figures 7.a, 8.a & 9.a, it can be seen that as the modulation depth increases, the time period of the pole-voltage is decreased (frequency is increased) because of V/f control.

It was mentioned earlier (also evident from Figs.4 and 5) that with the proposed CO-PD-SPM, the number of switchings has increased which is the main drawback. The normalized harmonic spectra of the motor phase voltage using the PWM switching strategies proposed in this paper i.e. CO-PD-SPWM and also the conventional PD-SPWM are shown in Fig.10 for critical comparison (all with f_1=20Hz). Though the number of switchings increases, it is evident from Fig.10.b that there is an improved phase voltage harmonic spectra with the use of the proposed CO-PD-SPWM method.

Hence, it demonstrated that the six-level diode-clamped inverter is capable of generating multiple levels in its output by changing the modulation depths or the frequency of the modulating signal (Figs. 7.a, 8.a and 9.a). The principal advantage with this PWM scheme in fact is improved spectral performance as compared to the conventional PWM scheme even though the resulting switchings are more. The results with the CO-PD-SVPWM scheme proposed for the six-level diode clamped inverter with the fundamental frequency of 20Hz is presented in Fig.11.

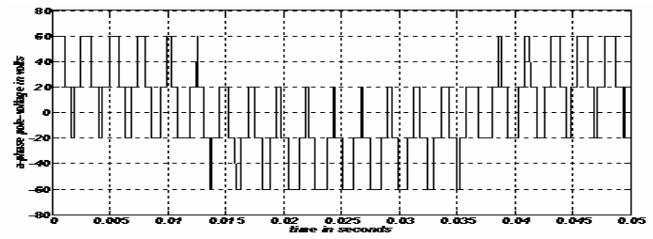


Fig. 7.a A-phase pole-voltage with f_1=20Hz.

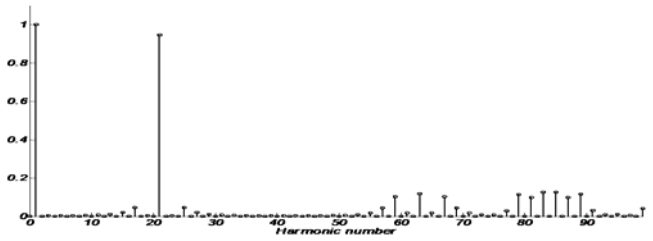


Fig. 7.b Normalized harmonic spectrum of a-phase pole voltage with f_1=20Hz.

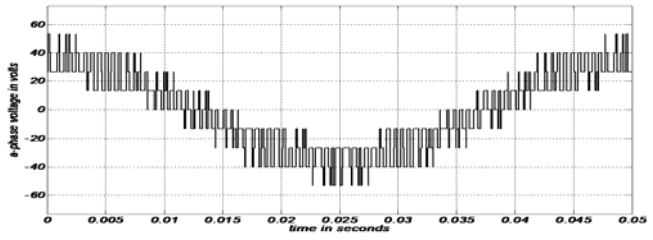


Fig. 7.c A-phase phase voltage with f_1=20Hz.

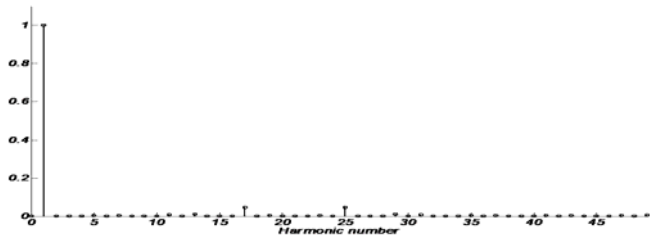


Fig. 7.d Normalized harmonic spectrum of the phase voltage with f_1=20Hz.

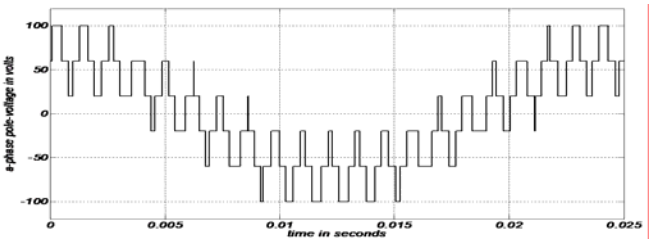


Fig. 8.a A-phase pole-voltage with f_1=40Hz.

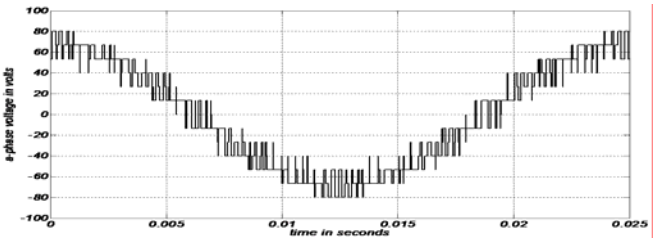


Fig. 8.b A-phase phase voltage with f_1=40Hz.

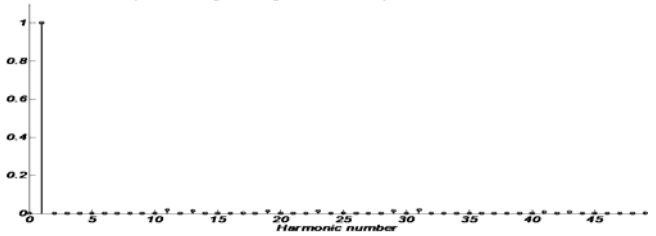


Fig. 8.c Normalized harmonic spectrum of the phase voltage with f_1=40Hz.

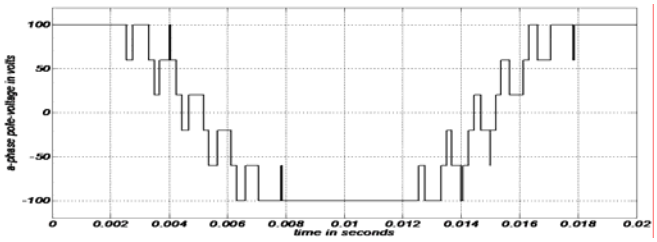


Fig. 9.a A-phase pole-voltage with over-modulation.

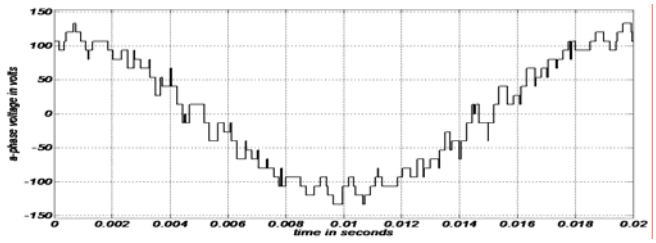


Fig. 9.b A-phase phase voltage with over-modulation.

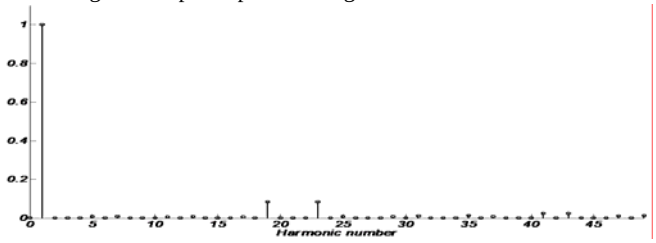
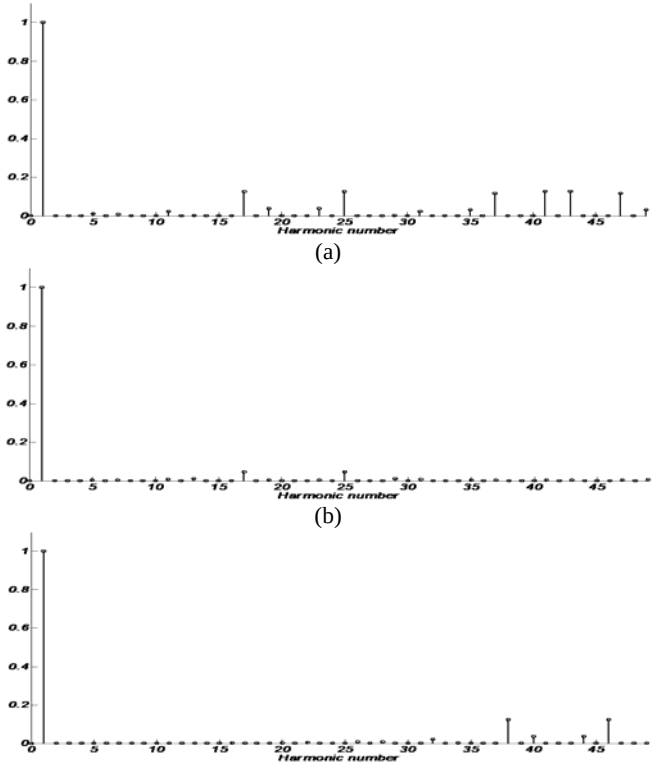
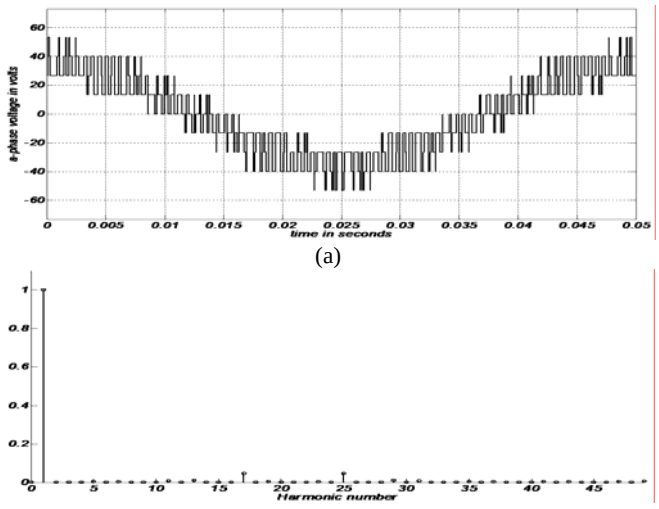


Fig. 9.c Normalized harmonic spectrum of the phase voltage with over-modulation



(a) (b) (c)

Fig. 10 Normalized harmonic spectra of the phase voltage with f_1=20Hz.using (a) conventional PD-SPWM (b) CO-PD-SPWM proposed in this paper & (c) conventional PD-SPWM and double the switching frequency



(a) (b)

Fig. 11.(a) A-phase phase voltage (b) Normalized harmonic spectrum of the a-phase voltage using the CO-PD-SVPWM proposed in this paper with f_1=20Hz.

VI. Conclusion

In this paper, uniform zero phase shifted carrier-overlapped multilevel PWM scheme are proposed for a six-level diode-clamped inverter topology. The overlapped carrier, sub-harmonic or CO-PD-SPWM and also CO-PD-SVPWM methods are presented to control the six-level diode-clamped inverter switches demonstrating the multiple levels obtained from the inverter. The principle difference between the conventional PD-SPWM and the CO-PD-SPWM is also discussed and presented. Through simulation studies, it is demonstrated that the harmonic profile of the phase voltage of the inverter improves with the use of CO-PD-SPWM scheme proposed in this paper as compared to the use of the conventional PD-SPWM, suggesting that the THD in the output voltage can be reduced. Also, results with the carrier-based CO-PD-SVPWM are presented that can be used to improve the DC-bus utilization. Hence, with the proposed carrier-overlapped PWM scheme, though it is seen that the number of switchings are increased, it in fact facilitates an improved spectral performance of the motor phase voltage especially at low speeds of operation of the motor. This aspect of the proposed PWM scheme can be exploited in high power applications requiring low speeds of operation of the drive.

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