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CMOS-Compatible Silicon Nanoplasmonics for On-Chip Integration

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***Abstract*—**Although silicon photonic devices provide a significantly larger bandwidth and dissipate a substantially less power than the electronic devices, they suffer from a large size due to the fundamental diffraction limit and the weak optical response of Si. A potential solution is to exploit Si plasmonics, which may not only miniaturize the photonic device far beyond the diffraction limit, but also enhance the optical response in Si due to the electromagnetic field confinement. In this paper, we discuss and summarize the recently developed metal-insulator-Si-insulator-metal nanoplasmonic waveguide as well as various passive and active plasmonic components based on this waveguide, including coupler, bend, power splitter, ring resonator, MZI, modulator, detector, etc. All these plasmonic components are CMOS compatible and could be integrated with electronic and conventional dielectric photonic devices on the same SOI chip. More potential plasmonic devices as well as plasmonic nanocircuits with complex functionalities are also addressed.

***Keywords*—**Silicon nanoplasmonics, Silicon nanophotonics, On-chip integration, CMOS

I. Introduction

SILICON electronic circuits have continuously scaled in integration density and switching speed to keep pace with Moore's law. For instant, the International Technology Roadmap for Semiconductors predicts that the chip capacities will increase to 1 Tbit and the transistor gate length will be reduced to 4.5 nm by 2022. Two of the most daunting problems to achieve this goal are thermal and single delay issues associated with electronic interconnections. Optical interconnects which provide a significantly larger bandwidth and dissipate a substantially less power than the electronic interconnections may offer solutions for circumventing these problems. Si photonics may be integrated with electronics on the same chip to achieve the so-called electronic-photonic integrated circuits (EPICs). Unfortunately, dielectric photonic components suffer from a large, wavelength-scale size due to the fundamental diffraction limit and the weak optical response of Si. Therefore, a major challenge of the state-of-the-art Si EPICs is the miniaturization of optical components beyond the diffraction limit in order to bridge the dimension mismatch between the electric and optical components.

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A potential solution for this challenge is to utilize surface plasmon polaritons (SPPs) excited at the metal-dielectric interfaces [1-3]. A SPP guiding structure (namely, a plasmonic waveguide), which comprises one or more metal-dielectric interfaces, is a basic platform to link various integrated functional plasmonic components to a plasmonic nanocircuit.

However, due to the unavoidable resistive damping in the metals, the plasmonic waveguides which can tightly confine the mode in subwavelength dimensions exhibit a larger propagation loss (usually in the dB/μm scale) than the conventional Si waveguides (usually in the dB/cm scale).

Therefore, the plasmonic components are not expected to replace the optical counterparts in the EPICs, but are expected to additionally implement in the EPICs to realize a wide range of functionalities that are difficult, inefficient, or impossible to be realized based on the conventional Si waveguides. Namely, the next-generation EPICs will be the integration of all electronic, photonic, and plasmonic components in the same chip [4-5].

An ideal plasmonic waveguide should meet the following two requirements: (1) better tradeoff between the light confinement and the propagation distance; and (2) CMOS compatible for seamless integration in the existing EPICs.

Many types of plasmonic waveguides as well as plasmonic waveguide components have been proposed and/or demonstrated in the past years, such as gap-SPP [6], hybrid [7], dielectric-loaded SPP waveguides [8], and many others. We regard that the recently developed horizontal metal-insulator-Si-insulator-metal nanoplasmonic waveguide [9-11] is an attractive candidate for seamless integration into the existing Si-EPICs. First, its lateral mode confinement is solely determined by the Si core width and the surrounding insulator thickness, which can be shrunk to nanometer scales using standard CMOS technology. Second, its propagation loss around 1550-nm telecom wavelengths is relatively low when Cu is used as the metal [10]. Third, it can link with the conventional Si waveguide through a simple tapered coupler with the coupling efficiency as high as 90% [10]. Fourth, various ultracompact passive components, such as power splitters [12], ring resonator [13], and Mach-Zehnder interferometers (MZIs) [11] can be easily realized based on the waveguide. Fifth, the Si core can be used as an active material for electro-optic modulation through the free-carrier dispersion effect in Si [14-15]. Sixth, a functional material, e.g., a dielectric with large thermo-optic, electro-optic, or nonlinear effect, can be readily inserted or replace the insulator between the Si core and the metal to introduce effective active functionalities because of the significant enhancement of the SPP field in this low-index dielectric layer.

One example of such a device is an effective ultracompact SPP detector, which has been theoretically proposed utilizing a suitable ultrathin silicide layer inserted between the insulator and the Si core [16]. Finally, it is fully CMOS compatible, enabling to be seamlessly implemented into the existing Si EPICs. In this paper, we review the recently developed various components based on the horizontal metal-insulator-Si-insulator-metal waveguide. New potential devices such as thermal optical devices as well as plasmonic nanocircuits with complex functionalities are also discussed.

II. Basic Structure of the Nanoplasmonic Waveguide

Fig. 1 (a) shows the schematic structure of the metal-insulator-Si-insulator-metal nanoplasmonic waveguide (PWG) studied in this work. The PWG with length of L_g and width of W_p is inserted in a conventional Si waveguide with width of W_{Si} through two identical tapered couplers with length of L_c. The Si core of PWG along with Si waveguides is defined by the standard ultraviolet lithography and dry etch process. By varying the layout of the Si core, various passive devices such as bends, rings, and MZIs can be fabricated with the same process flow, as described below. Fig. 1(b) is a microscopy picture of a final plasmonic device. The metal covered plasmonic device is inserted in the Si waveguide network.

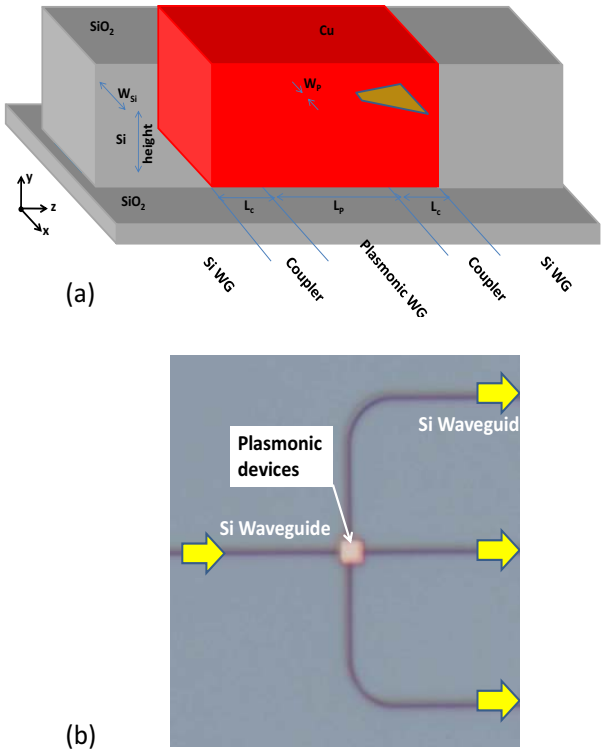

Fig. 1 (a) Schematic view of horizontal metal-insulator-Si-insulator-metal nanoplasmonic waveguide studied in this work. The Si core of with width of W_P and length of L_p is linked with conventional Si channel waveguides with width of W_{Si} through two identical tapered couplers with length of L_c; (b) the fabricated chip showing that the metal-covered plasmonic devices are inserted in the conventional Si waveguides

III. Fabrication Flow and the Measurement Setup

The devices are fabricated using the standard Si CMOS technology on silicon-on-insulator (SOI) substrates. The main steps of fabrication flow are shown in Fig. 2 schematically. The scanning electron microscopy (SEM) images after step (b) and step (d) are shown in Fig. 3(a) and (b), respectively. The cross-sectional transmission electron microscopy (XTEM) image of the final device is shown in Fig. 3(c). The Si core has a narrow width of several tens of nanometers, and it can be further reduced using the standard CMOS technology. The insulator here is thermal oxide, whose thickness can be precisely controlled. Moreover, this layer can be readily replaced by other functional dielectric material for various active plasmonic devices.

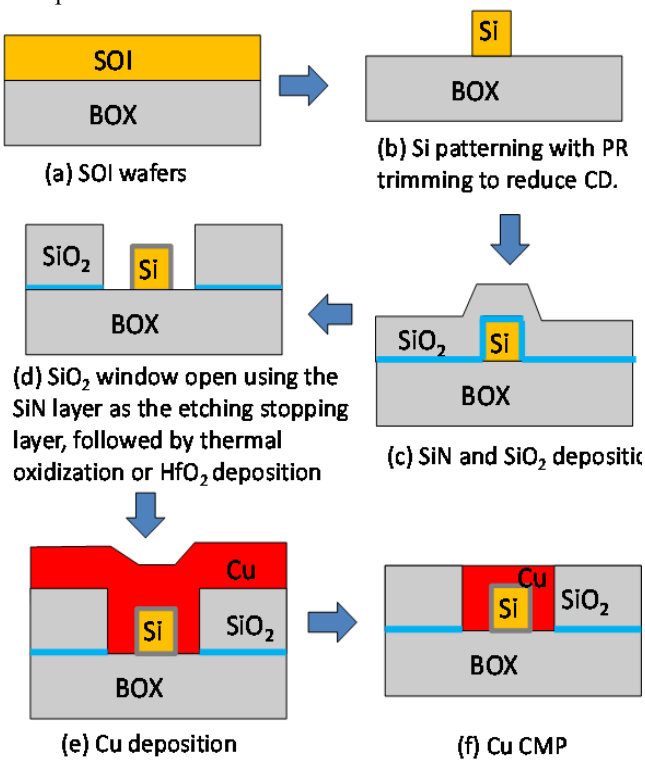

Fig. 2 Some main steps for fabricating passive metal-insulator-Si-insulator-metal nanoplasmonic waveguide components, here, Cu is used as the metal and thermal oxide is used as the insulator, they can be replaced by other metal or other dielectric materials readily, such as HfO_2, TiO_2, etc

The diced chips are characterized using standard fiber-to-fiber measurement setup. Quasi-TE-polarized light (the electric field is parallel to the chip surface plane) from an Expo broad-band laser source, whose spectral range is ~1520–1620 nm, is coupled into the input Si waveguide through a lensed polarization-maintaining (PM) sing-mode fiber. Light transmitted from the output Si waveguide is coupled to another single-mode fiber and is measured by a power meter and an AQ6317B optical spectrum analyzer (OSA). A semi-auto micrometer piezo-stage is used to adjust the fibers to search the maximum output power.

A commercial software FullWAVE/RSOFT [17] is used for three-dimensional (3D) finite-difference time-domain (FDTD) simulation. The Si core is approximated to an ideal 340-nm-high rectangle on the SiO_2 substrate, surrounded by a uniform thermal SiO_2 layer. 1550-nm TE light is launched at the input 500-nm-wide Si channel waveguide and transports into the plasmonic waveguide through a 1-μm-long tapered coupler. The detailed settings for the 3D FDTD simulation have been described elsewhere [10]. The refractive indices of Si and SiO_2 at 1550 nm are set to 1.445 and 3.455, respectively, and the Cu complex permittivity is ~ -122+6.2*i* at 1550 nm [18].

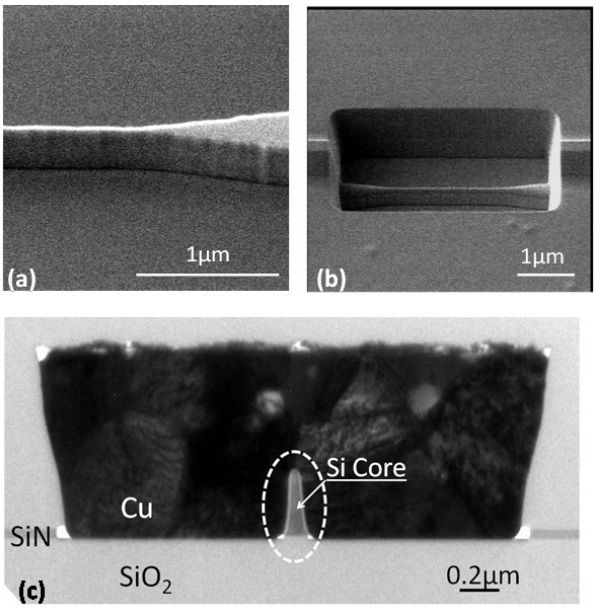

Fig. 3 (a) SEM image of the Si core of the plasmonic waveguide; (b) SEM image showing SiO_2 window where Cu will be filled in; (c) XTEM image of the final structure

IV. Experimental Results

A. Straight waveguides

Fig. 4 show the transmission power measured on the straight plasmonic waveguides with length (L_P) ranging from 1 to 100 μm, normalized by that measured from the reference waveguide (i.e., the Si waveguide without the plasmonic area). The transmitted power exhibits a good linearity with L_P. The slope of the linearly fitting lines gives the propagation loss of ~0.281, ~0.286, ~0.287, and ~0.304 dB/μm for the plasmonic waveguides with W_P of ~102, ~94, ~81, and ~64 nm, respectively, in good agreement with those predicted from the 3-D FDTD simulation. The y-intercept gives the coupling loss of the 1-μm-ling tapered coupler which links the 500-nm-wide Si strip waveguide and the plasmonic waveguide. The difference in the coupling loss of these four plasmonic waveguides is smaller than the experimental error. Therefore, the coupling losses obtained from all tested waveguides are averaged, which is ~0.51 dB/facet, corresponding to a coupling efficiency of ~89%. The propagation loss increases significantly if Al is used as the metal, which can be attributed to the larger imaginary part of Al permittivity than that of Cu.

Because the Cu permittivity depends on the fabrication condition, it implies that we may further reduce the propagation loss by optimization of the Cu deposition process.

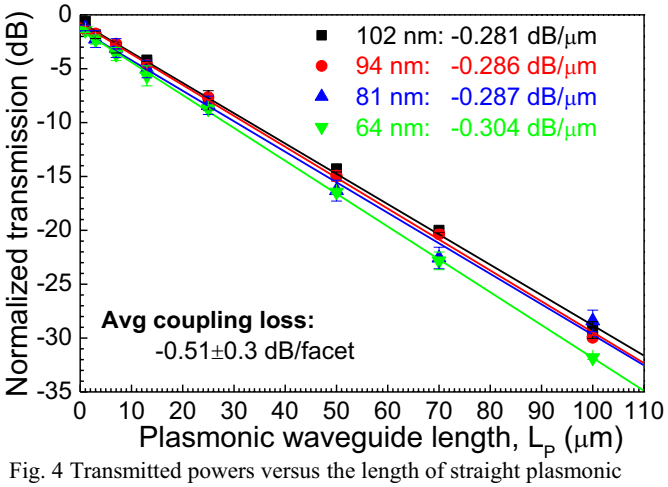

Fig. 4 Transmitted powers versus the length of straight plasmonic waveguides with different W_Ps, normalized by that measured from the reference waveguide without the plasmonic area. From linearly fitting, the propagation loss and the coupling loss can be extracted

B. Coupler between the plasmonic waveguide and the Si channel waveguide

Because the plasmonic waveguide has propagation loss several orders of magnitude larger than the Si waveguide, the plasmonic waveguide is not expected to replace the Si waveguide for long-distance optical signal transferring, but it will be used to address functional plasmonic devices. Therefore, an effective coupler is extremely important to link the plasmonic waveguide and the Si strip waveguide.

For the horizontal metal-insulator-Si-insulator-metal waveguide, there exists a simple tapped coupler, as shown in Fig. 5. This is a significant benefit of the metal-insulator-Si-insulator-metal plasmonic waveguide. Fig. 5(a) depicts the top-view E_x-field distribution in the case of L_c = 1 μm and W_p = 100 nm, showing power launched in the Si waveguide is gradually transferred and concentrated in the sidewall thin SiO_2 layer of the PWG through the tapered coupler.

Fig. 5(b) shows the theoretical and experimental coupling losses between the 500-nm-wide Si waveguide and the Cu/SiO_2(12 nm)/$Si(W_p)$/SiO_2(12 nm)/Cu PWG as a function of the tapered coupler length.

The coupling loss is mainly caused by two sources. One is the reflection at the Si-waveguide/coupler and coupler/PWG interfaces and the other is the propagation loss along the taper coupler. The reflection loss dominates for the shorter L_C coupler. For the extreme case of L_C = 0 (i.e., direct coupling), simulation indicates that the reflection ratio increases from ~20% to ~69% with W_P decreasing from 200 nm to 20 nm.

The coupling efficiency increases with L_C increasing, reaching a maximum of ~ -0.2 dB at L_C = ~0.3–0.5 μm, and then decreases with L_C further increasing due to the increase of the predominant propagation loss along the coupler. The experimental coupling loss agrees well with the theoretical values.

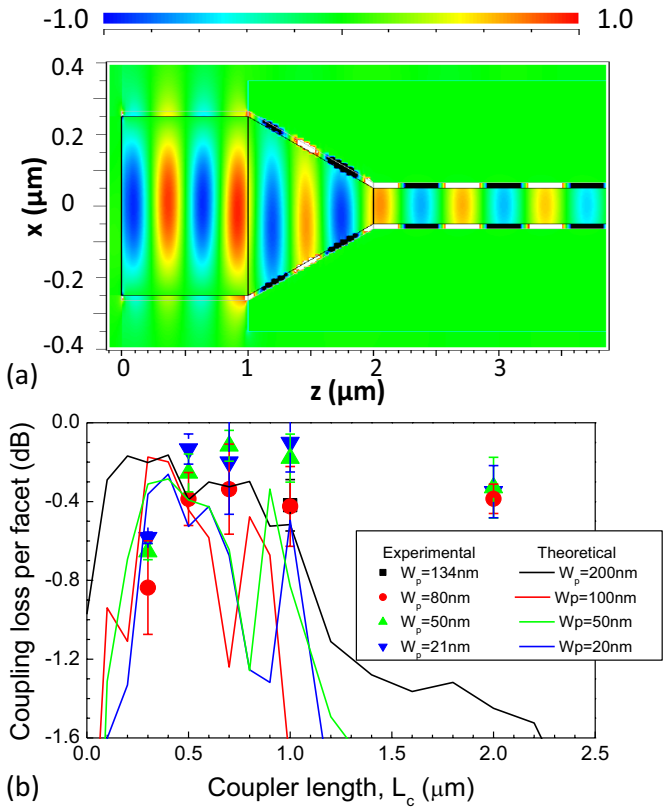

Fig. 5 (a) Top-view of the calculated $E_x(x,y)$ distribution in the case of L_c = 1 μm and W_p = 100 nm; (b) Theoretical and experimental coupling losses between the 500-nm-wide Si waveguide and Cu-SiO_2(12 nm)-Si(W_p)-SiO_2(12 nm)-Cu PWG with various W_Ps as a function of the tapered coupler length, L_C

C. Sharp 90° bends

The plasmonic waveguide supports sharply bending with a relatively low loss, thus enabling to route SPP signals flexibly in plasmonic nanocircuits. To measure the pure bending loss accurately, bent plasmonic waveguides with multiple sharp 90° bends are fabricated, as shown in Figs. 6 (a)-(f), which contains 2, 4, 6, 8, 10, and 12 sharp 90° bends, respectively, and with the total plasmonic waveguide length of 13 μm. Fig. 6(g) depicts the transmitted powers as a function of bend number, normalized by the corresponding 13-μm-long straight plasmonic waveguide. Due to the reflection-induced Fabry-Perot effect, the linearity of the normalized power versus the bend number is poor, making it difficult to extract the bending loss accurately. Nevertheless, a linearly fitting for all data points gives an approximate bending loss of ~0.73±0.06 dB/turn. For comparison, the bending loss predicted from the 3D FDTD simulation is 0.77 dB/μm.

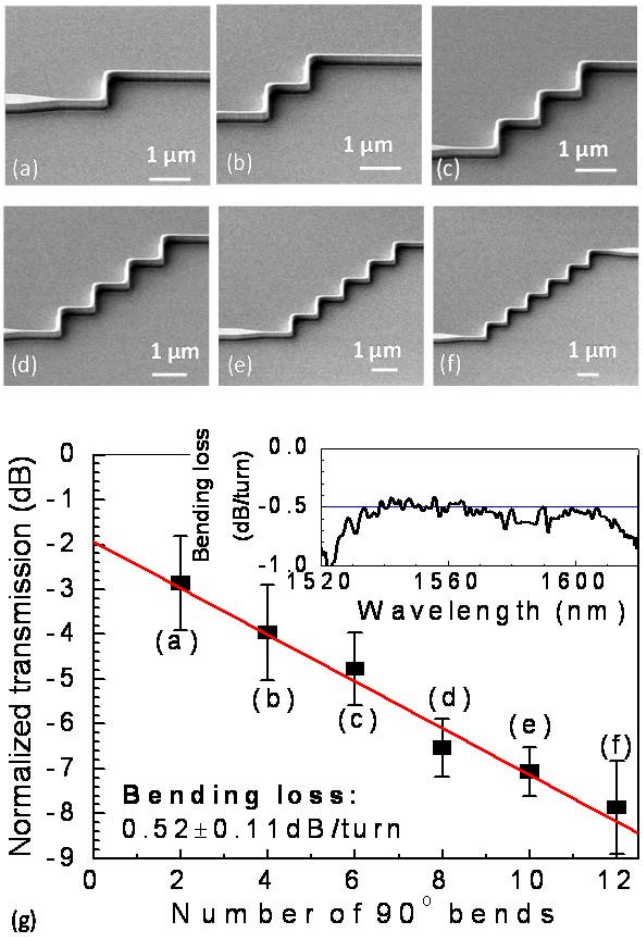

Fig. 6 (a)-(f) SEM images (the Si core patterns) of a set of bent plasmonic waveguides containing 2, 4, 6, 8, 10, and 12 sharp 90° bends, respectively, the total plasmonci waveguide length is 13 μm; (g) Transmitted powers measured on bent plasmonic waveguides as a function of the number of bends, normalized by the corresponding 13-μm-long straight plsmonic waveguide. The inset is the wavelength dependence of the bending loss

D. Power splitters

The Cu-SiO_2-Si-SiO_2-Cu plasmonic waveguides support large-angle power splitting with relatively low excess loss. Figs. 7(a), (c) and (e) shows SEM images of symmetric 1×2 and 1×4 splitters with a 90° open angle and 1×2 T-splitter, respectively. The total length of each plasmonic route is 3 μm. The corresponding measurement results on these devices are shown in Figs. (b), (d), and (f), respectively.

We can see that the spectra are almost wavelength independent and the difference among different output ports in the splitters is within the measurement error, confirming the symmetric nature of our splitters. To reduce the experimental uncertainty, three identical splitters are measured.

The averaged output power after subtracting that measured on the 3-μm-long straight plasmonic waveguide is -3.8±0.4 dB for the 1×2 splitter and -7.5±0.2 dB for the 1×4 splitter. Both are in good agreement with the simulation results. The experimental excess loss for one Y-splitter is estimated to be ~0.74 dB. The splitters with larger W_Ps are also examined. They exhibit similar splitting behaviors (not shown here).

The apparent insensitivity of the excess loss on W_P may also be attributed to the relatively thick SiO_2 layer, as the above-observed apparent insensitivity of the pure bending loss on W_P. For the T-splitter, on the other hand, the experimental excess loss is larger than that predicted from the 3D FDTD simulation, which may be attributed to the enlarged junction, as shown in Fig. 7(e).

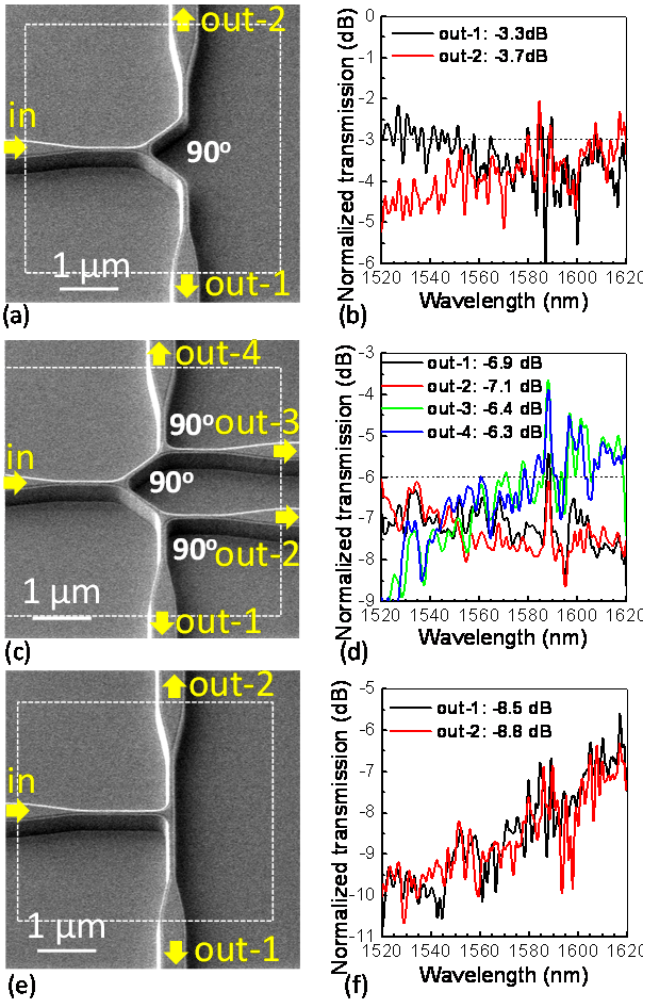

Fig. 7 (a) SEM image (the Si core pattern) of a symmetric 1×2 splitter with 90° opening angle; (b) The spectra measured from output ports of a 1×2 splitter with 64-nm W_P, normalized by that measured on a corresponding 3-μm-long straight plasmonic waveguide. (c)-(d) are the corresponding figures for a symmetric 1×4 splitter. (e)-(f) are the corresponding figures for a symmetric 1×2 T-splitter

E. Mach-Zehnder interferometers

MZI is a basic building block for many optical devices. Fig. 8(a) shows schematically a typical design of an ultracompact plasmonic MZI, where the opening angle of the splitter and the combiner is 120°, the upper oblique arm is 1-μm long, and the bottom oblique arm is (1 + ΔL)-μm long. ΔL varies from 0 to 0.8 μm with a step of 0.1 μm. The input plasmonic waveguide before splitting and the output plasmonic waveguide after combing are both 1-μm long.

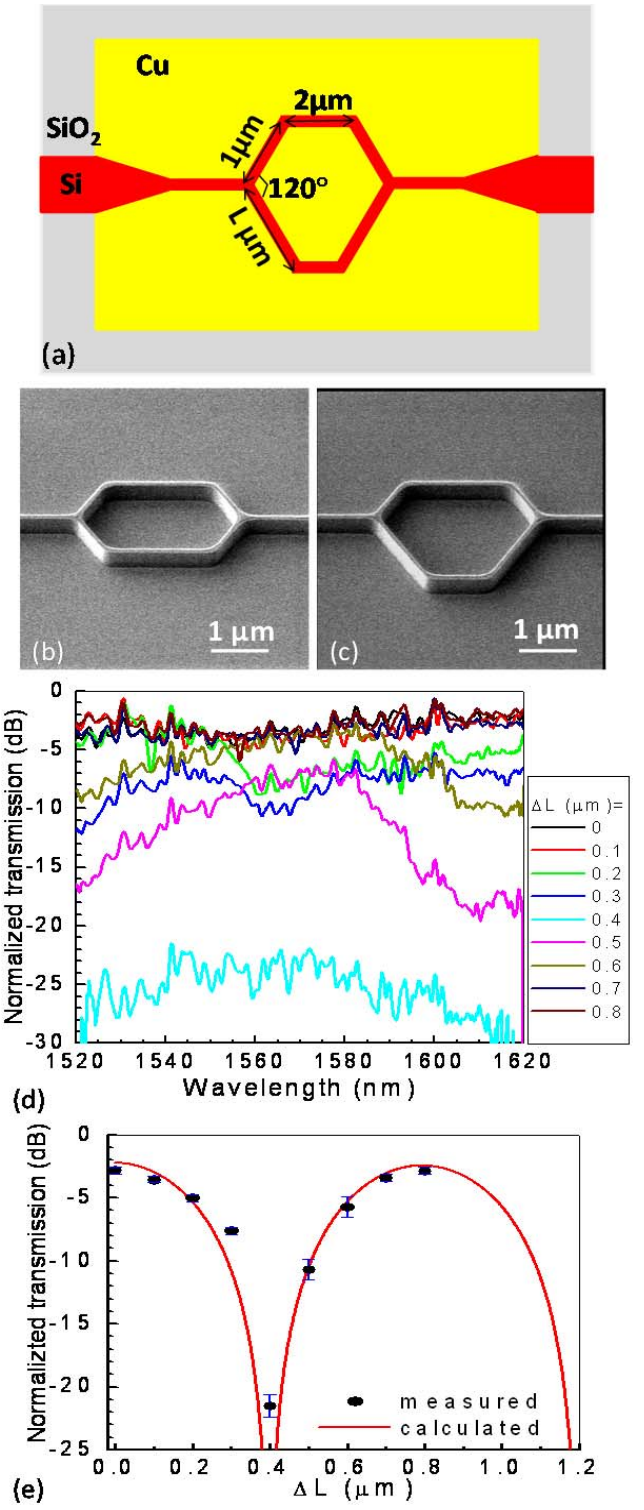

Fig. 8 (a) Schematic top view of plasmonic MZIs designed in this work, ΔL varies from 0 to 0.8 μm with a step of 0.1 μm; (b)-(c) SEM image (Si core pattern) of MZI with ΔL = 0 and ΔL = 0.8 μm; (d) The normalized transmission spectra measured on MZIs with ΔL of 0, 0.1, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, and 0.8 μm, respectively; and (e) The transmitted powers as a function of ΔL, as well as the fitting curve based on Eq. 1 with the best fitting parameters of $\alpha_1 = 0.69$ and $n_{eff} = 1.85$

Therefore, the total plasmonic route through the upper arm is 6 μm, and that through the bottom arm is (6 + ΔL) μm. Figs. 8 (b) and (c) show SEM images of the MZIs with ΔL = 0 and 0.8 μm, respectively. Fig. 8(d) depicts the measured transmission spectra of a set of MZIs, normalized by the 6-μm-long straight plasmonic waveguide. The transmission spectrum of the balanced MZI (i.e., ΔL = 0) is wavelength independent, whereas the spectra of the unbalanced MZIs (i.e., ΔL ≠ 0) become wavelength dependent, especially in the case of ΔL = 0.4 μm. But, no clear peak can be observed in the spectra due to the large free spectral range (FSR, = $\lambda_r^{\,2}/(n_{eff}\Delta L)$) and the narrow spectral range (~1.52-1.62 μm) of our measurement setup. Fig. 8(e) plots the measured normalized transmitted powers as a function of ΔL, which can be fitted by the following equation:

$$T(\lambda)=\frac{1}{4}\cdot\alpha_1\left[1+\alpha_2^{\,2}+2\cdot\alpha_2\cdot\cos\left(\frac{2\cdot\pi}{\lambda}\cdot n_{eff}\cdot\Delta L\right)\right] \quad (1)$$

where α_1 is the normalized transmission loss due to splitting, combining, and bending. α_2 (= $10^{-\alpha/10\times\Delta L}$, where α is the propagation loss in dB/μm unit) is the power difference after propagating through two arms. The best fit parameters are found to be α_1 = 0.69 and n_{eff} = 1.85, which agrees well with that extracted from the 3D FDTD simulation of the straight plasmonic waveguides.

F. Waveguide-ring resonators

Waveguide-ring resonator (WRR) plays an important role in the success of Si photonics. For a conventional WRR based on Si waveguides, efficient coupling between the ring and bus waveguides is achieved through an evanescent optical field in the gap separating them. This gap is typically in the range of 200–500 nm. However, the gap should be less than ~26 nm to achieve a noticeable evanescent coupling for a WRR based on metal-insulator-metal (MIM) type plasmonic waveguides because the penetration depth of electrical field in metal is only ~26 nm. Such a narrow gap is very difficult to realize even with state-of-the-art electron-beam or ion-beam lithography. To circumvent this problem, an aperture coupler has been proposed theoretically for MIM plasmonic WRRs [19] and has been experimentally realized for dielectric-loaded plasmonic WRRs [20]. Here, we design a metal-insulator-Si-insulator-metal plasmonic waveguide WRR as schematically shown in Fig. 9(a). Fig. 9(b) is the SEM image of the Si core of the WRR with radius of 0.91 μm, showing a small aperture to link the bus and ring waveguides. Fig. 9(c) plots the normalized transmission spectrum, T(λ), of a plasmonic WRR with R = 0.91 μm and L_P = 3 μm, measured from the devices with and without the ring. The normalized spectrum is fitted by the following well-known analytical expression:

$$T(\lambda)=\frac{\alpha^2+|t|^2-2\alpha|t|\cos\left(4\pi^2 n_{eff}R/\lambda-\phi\right)}{1+\alpha^2|t|^2-2\alpha|t|\cos\left(4\pi^2 n_{eff}R/\lambda-\phi\right)} \quad (2)$$

where α and t (=$|t|\exp(i\phi)$) are related to the field attenuation due to propagation along the ring and coupling between the bus and the ring waveguide, respectively.

The fitting parameters are t, n_{eff}, and ϕ, while R = 0.91 μm and α = 0.59 are fixed and calculated from the measured propagation loss. The best fit values are found to be t = 0.57, ϕ = -0.6°, and n_{eff} = 1.95. The n_{eff} value agrees remarkably well with that calculated from the straight plasmonic waveguide. Fig. 9(c) shows only one resonance at λ_r = 1596 nm in the range between 1520 and 1620 nm, which corresponds to the 7th-order resonance, obeying the relation of $4\pi^2 n_{eff}R/\lambda_r-\phi=2\pi m$ (where m is an integer). The cavity mode volume (V) is calculated to be ~0.145 μm^3. The WRR has insertion loss (IL, the maximum normalized transmission) of ~2.4 dB, extinction ratio (ER, the maximum-to-minimum transmission ratio) of ~28 dB, and FSR (= $\lambda_r^{\,2}/(n_{eff}2\pi R)$) of ~143 nm.

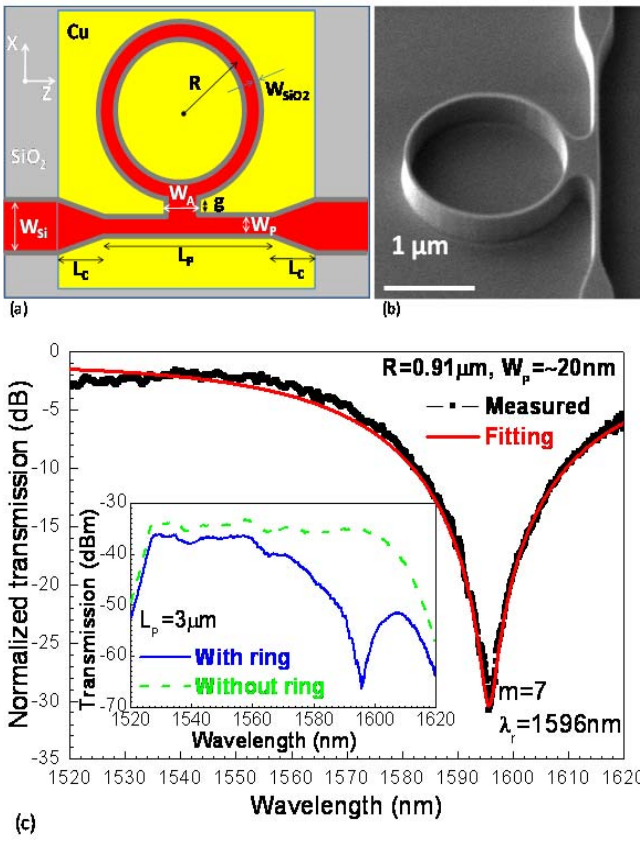

Fig. 9 (a) Schematic top view of plasmonic WRR designed in this work, (b) SEM image (Si core pattern) of WRR with R of 0.91 μm; (c) The normalized transmission spectra measured on the WRR, the inset is the raw spectra measured on the devices with and without the ring

G. Ultra-compact electro-absorption modulators

The metal-insulator-Si-insulator-metal structure is naturally a MOS structure, thus an ultracompact EA modulator can be designed, which relies on a highly accumulated electron layer at the insulator/Si interface induced by an applied voltage. Proof-of-concept devices are designed as shown in Figs. 10 (a) and (b), and are fabricated using standard CMOS technology. Fig. 10(c) is the microscopy picture of the fabricated EA modulator.

Fig. 11(a) shows the normalized output spectra (i.e., after subtracting the spectrum measured from a reference Si-waveguide without the plasmonic structure) measured on a device with L_P = 3 μm with an applied voltage ranging from 0 to 7 V. Larger voltages will break down the gate oxide. We see that the transmitted power decreases substantially as the voltage increases when V is larger than ~4 V. The almost wavelength-independent modulation reflects the broadband nature of the EA modulator. The normalized output powers at 1550 nm are depicted in Fig. 11(b) as a function of voltage for devices with different L_Ps. At low voltages (e.g., < ~4 V), the modification is very small, whereas it increases significantly when the voltage becomes larger. A 3-dB modification is obtained at ~6.5 V bias for the device with L_P = 3 μm (thus the total length including two tapered couplers is 4 μm). As expected, a longer device provides a larger optical modification at the same voltage.

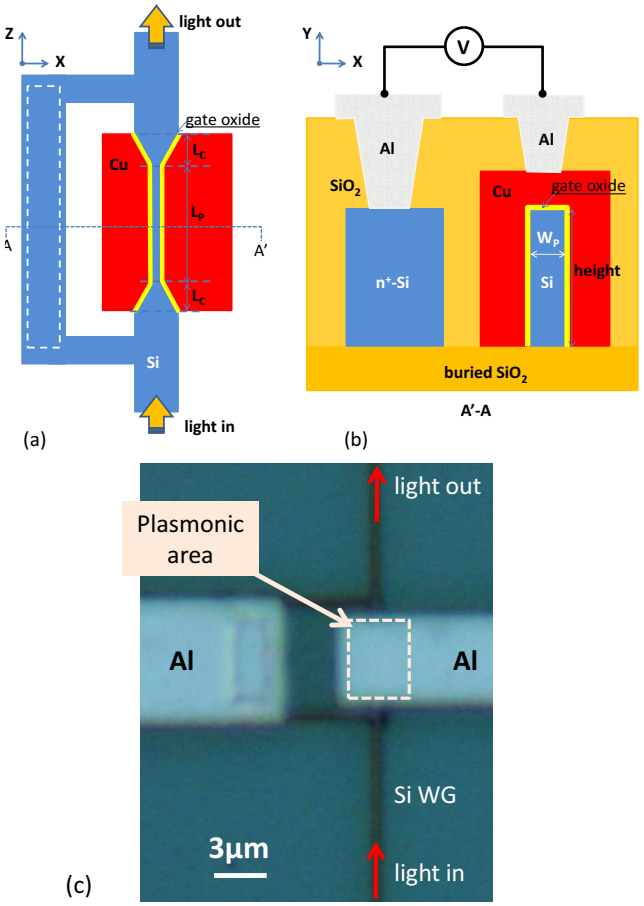

Fig. 10 (a) Schematic top view of a proof-of-concept Si nanoplasmonic EA modulator, (b) Schematic cross-sectional view along A-A', and (c) the microscopy picture of the fabricated EA modulator

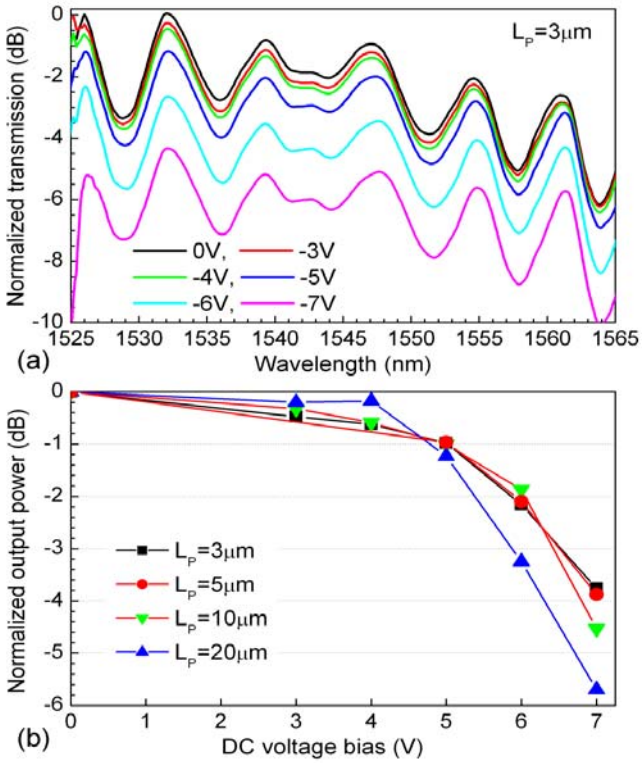

Fig. 11 (a) The normalized transmission spectra measured on a device with L_P = 3 μm applied by different voltages; (b) The normalized output power at 1550 nm as a function of the applied voltage for devices with L_P of 3, 5, 10, and 20 μm

V. Conclusion

In this paper, the recently developed metal-insulator-Si-insulator-metal plasmonic waveguides as well as various passive and active components based on the waveguide are discussed. The straight waveguide with Cu as the metal exhibits a relatively low propagation loss. Moreover, the plasmonic waveguide can effectively couples with the conventional Si strip waveguide though a simple tapper coupler, which makes it easy for implementation in the Si waveguide network. The waveguides support sharp 90° bend with a relatively low bending loss of ~0.73 dB/turn. Owing to the low bending loss, various ultracompact power splitters and MZIs can be flexibly designed for plasmonic nanocircuits. The fabricated 1×2 Y-splitter has excess loss of ~0.74 dB and MZIs has normalized insertion loss of ~1.7 dB and extinction ratio of ~18 dB, in good agreement with those predicted from the 3D FDTD simulation.thus a series of passive components such as bends, power splitters, and MZIs can be designed and fabricated. A small aperture is necessary to design and fabricate WRRs because of the tight field confinement in the plasmonic waveguide. A plasmonic WRR with sub-micrometer radius has been demonstrated with high performance. Moreover, active devices such as EA modulator are also demonstrated, although many optimizations are necessary to improve their performance. The above results indicate that the metal-insulator-Si-insulator-metal plasmonic waveguide is an active platform for CMOS-compatible Si plasmonic nanocircuits for on-chip integration.

REFERENCES

[1] M. Dragoman and D. Dragoman, "Plasmonics: applications to nanoscale terahertz and optical devices," Prog. Quant. Electron. **32**(1), 1-41 (2008).
[2] D. K. Gramotnev and S. I. Bozhevolnyi, "Plasmonics beyond the diffraction limit," Nat. Photonics **4**, 83-91 (2010).
[3] R. F. Oulton, G. Bartal, D. F. P. Pile, and X Zhang, "Confinement and propagation characteristics of subwavelength plasmonic modes," New J. of Phys. **10**, 105018 (2008).
[4] E. Ozbay, "Plasmonics: merging photonics and electronics at nanoscale dimensions," Science **311**(5758), 189-193 (2006).
[5] R. Zia, J. A. Schuller, A. Chandran, and M. L. Brongersma, "Plasmonics: the next chip-scale technology," Mater. Today **9**(7-8), 20-27 (2006).
[6] S. I. Bozhevolnyi and J. Jung, "Scaling for gap plasmon based waveguides," Opt. Express **16**(4), 2676-2684 (2008).
[7] R. F. Oulton, V. J. Sorger, D. A. Genov, D. F. P. Pile, and X Zhang, "A hybrid plasmonic waveguide for subwavelength confinement and long-range propagation," Nat. Photonics **2**, 496-500 (2008).
[8] T. Holmgaard and S. I. Bozhevolnyi, "Theoretical analysis of dielectric –loaded surface plasmon-polariton waveguides," Phys. Rev. B 75, art. 245405 (2007).
[9] S. Y. Zhu, T. Y. Liow, G. Q. Lo, and D. L. Kwong, "Fully complementary metal-oxide-semiconductor compatible nanoplasmonic slot waveguides for silicon electronic photonic integrated circuits," Appl. Phys. Lett. **98**, art. 021107 (2011).
[10] S. Y. Zhu, T. Y. Liow, G. Q. Lo, and D. L. Kwong, "Silicon-based horizontal nanoplasmonic slot waveguides for on-chip integration," Opt. Express **19**, 8888-8902 (2011).
[11] S. Y. Zhu, G. Q. Lo, and D. L. Kwong, "Components for silicon plasmonic nanocircuits based on horizontal Cu-SiO_2-Si-SiO_2-Cu nanoplasmonic waveguides," Opt. Express **20**, 5867-5881 (2012).
[12] S. Y. Zhu, G. Q. Lo, and D. L. Kwong, "Nanoplasmonic power splitters based on the horizontal nanoplasmonic slot waveguide," Appl. Phys. Lett. **99**, art. 031112 (2011).
[13] S. Y. Zhu, G. Q. Lo, and D. L. Kwong, "Experimental demonstration of horizontal nanoplasmonic slot waveguide-ring resonators with submicron radius," IEEE Photonic Techn. Lett. **23**(24), 1896-1898, (2011).
[14] S. Y. Zhu, G. Q. Lo, and D. L. Kwong, "Theoretical investigation of silicon MOS-type plasmonic slot waveguide based MZI modulators," Opt. Express **18**, 27802-27819 (2010).
[15] S. Y. Zhu, G. Q. Lo, and D. L. Kwong, "Electro-absorption modulation in horizontal metal-insulator-silicon-insulator-metal nanoplasmonic slot waveguides," Appl. Phys. Lett. **99**, art. 151114 (2011).
[16] S. Y. Zhu, G. Q. Lo, and D. L. Kwong, "Theoretical investigation of silicon Schottky barrier detector integrated in horizontal metal-insulator-silicon-insulator-metal nanoplasmonic slot waveguide," Opt. Express **19**, 15843-15854 (2011).
[17] http://www.rsoftinc.com
[18] S. Roberts, "Optical properties of copper", Physical Review **118**(6), 1509-1518 (1960).
[19] Z. Han, V. Van, W. N. Herman, and P. T. Ho, "Aperture-coupled MIM plasmonic ring resonators with sub-diffraction modal volumes", Optics Express **17**(15), 12678-12684 (2009).
[20] T. Holmgaard, Z. Chen, S. I. Bozhevolnyi, L. Markey, and A. Dereux, "Dielectric-loaded plasmonic waveguide-ring resonators", Optics Express **17**(4), 968-2975 (2009).