World Academy of Science, Engineering and Technology
International Journal of Electrical and Computer Engineering
Vol:3, No:10, 2009

A Power Reduction Technique for Built-In-Self Testing Using Modified Linear Feedback Shift Register

Mayank Shakya and SoundraPandian. K. K

***Abstract*—**A linear feedback shift register (LFSR) is proposed which targets to reduce the power consumption from within. It reduces the power consumption during testing of a Circuit Under Test (CUT) at two stages. At first stage, Control Logic (CL) makes the clocks of the switching units of the register inactive for a time period when output from them is going to be same as previous one and thus reducing unnecessary switching of the flip-flops. And at second stage, the LFSR reorders the test vectors by interchanging the bit with its next and closest neighbor bit. It keeps fault coverage capacity of the vectors unchanged but reduces the Total Hamming Distance (THD) so that there is reduction in power while shifting operation.

***Keywords*—**Linear Feedback Shift Register, Total Hamming Distance, Fault Coverage, Control Logic

I. INTRODUCTION

POWER Dissipation is a challenging problem in today's System-on-Chips (SoC) Design and Test. In general, power dissipation of a system in test mode is more than that in normal mode. This is because a significant correlation exists between the consecutive test vectors applied during the circuit's normal mode of operation, whereas this may not be necessarily true for applied test vectors in test mode of operation. Low correlation between test vectors increases switching activity and eventually leads to power dissipation in the circuit.

Built-In Self Test (BIST) is the most suitable approach for low power testing as it provides a larger scope for low power techniques to be used. BIST uses an LFSR as test pattern generator (TPG). The LFSR generates all possible test vectors with the proper use of tap sequence. Furthermore the pseudorandom behavior of the LFSR reduces the correlation among test vectors which means that it can achieve high fault coverage in a relatively short run of test vectors.

Mayank Shakya is with the department of electronics and communication, Indian Institute of Information Technology, Design and Manufacturing Jabalpur, Madhya Pradesh-482 005, India.

SoundraPandian.K.K is with the department of electronics and communication, Indian Institute of Information Technology, Design and Manufacturing Jabalpur,Mehgawan,Dumna Airport Road, Jabalpur, Madhya Pradesh -482 005,India .phone: +91-9425155395, email: kpandian@iiitdm.in

However, this lack of correlation among test vectors substantially increases the Hamming distance among the vectors which leads to increased switching activity in the CUT. This often causes more power dissipation in test mode of operation. It is therefore required to find an optimum linear feedback shift register which, in-itself is power efficient and the test vectors generated as well, are power efficient i.e., they cause least switching activity when scanned in into a scan chain of CUT, without compromising the fault coverage.

II. PROLOGUE

Many low power testing techniques have been proposed. Several categories of low power testing techniques can be found in [3]. However, there are two broad categories namely External Testing and BIST. The External Testing techniques include the methodologies based on Automatic Test Pattern Generator (ATPG),Vector Reordering and architecture whereas the BIST include techniques based on LFSR, Test Scheduling, Circuit Partitioning and Reseeding.

However, the vector ordering can be used in BIST environment as well. In ordering techniques, the THD i.e. the sum of the hamming distances is minimized by modifying the order in which test vectors of a given test sequence are shifted into the CUT. The Travelling Salesman Algorithm (TSA) has been quite useful for ordering the test vectors. The test vector ordering has been useful in minimizing the hamming distance among test vectors and thereby reducing in average and peak power. [5] [7].

Reordering of test vectors does not affect the fault coverage as overall the same set of test vectors are applied, just their order is modified [6]. The paper [7] discussed about two methods used for reordering of test vectors in order to reduce the dynamic power dissipation during testing of combinational circuits. Two search methods, 2-opt heuristic and a genetic algorithm based approach has applied and results obtained for combinational circuits. These techniques can be applied during external testing or deterministic BIST as well.

In BIST, LFSR is an important module. Several modified versions of LFSR have been proposed which consume relatively little power. Gated clock design of LFSR is presented in [4]. In [2] a modified LFSR is proposed which swaps the bits according to a particularly chosen selection bit.

III. MOTIVATION

Motivation for the proposed work arises from two observations. First is that the literature available focuses upon ordering the test vectors after obtaining the test vector sequences form the LFSR. And other is LFSR can itself be power efficient if modified for the purpose.

The aim of the work is to design an LFSR which in itself is power efficient and the test vectors generated from it are also power efficient. That is the test vectors cause lesser switching when scanned in.

IV. PROPOSED METHODOLOGY

In the proposed approach, an LFSR has been designed such that it reorders the test vectors to minimize the switching activity and consumes little power as compared to conventional LFSR.

The switching units (flip-flops) of the LFSR toggle unnecessarily in the process of generating 2^n sequence when same bits are repeated for a particular set of test sequences. Therefore the non performing flip-flops are disabled for a particular time period. The flip-flops are disabled by asserting the clock signal to state '0'. The behavior of the switching unit is projected in the Table.1

TABLE I TRUTH TABLE FOR THE MODIFIED CLOCK

Data_in	Data_out	Clock	Modified clock
1	0	1	1
0	1	1	1
1	1	1	0
0	0	1	0

The truth table logic can be realized by the use of an XOR and a NOR gate as shown in the figure.1

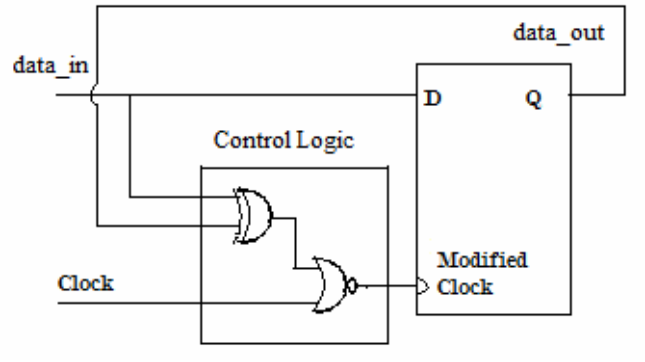

Fig. 1. Switching unit of LFSR with Modified Clock.

The CL logic shown in figure 1 can be used with each LFSR cell without modifying its tap sequence and thus without changing its behavior. Thus the clock signal is modified in order to reduce power consumption.

Let the hamming distance test vector V_i and V_{i+1} be $D(V_i, V_{i+1})$ which is the total number of changes between the vectors V_i and V_{i+1}. Then the Total Hamming Distance (THD) [9] can be calculated from the Equation (1)

$$THD = \sum_{i=1}^{i=n+1} D(Vi, Vi+1) \quad (1)$$

The THD is the measure of changes occurring among the test vectors. These changes determine the amount of switching activity in a CUT. The THD can be minimized if test vectors are shifted in a proper order. The LFSR with control logic is used along with a reordering algorithm based on bit interchanging method in [5]. In an n-bit LFSR with bits 1, 2, 3, 4…q, q+1, n, if the bit n (the selection bit) has a value '0' (or '1') the interchanging is performed between bit 1 & bit 2, between bit 3 & bit 4 and so on. If bit n has a value of 1(or 0) then no interchanging is performed. The process ultimately generates a new order of test vectors.

Let us illustrate the point with an example. We have a set of test vectors generated from a maximal length 3-bit LFSR. Applying the bit interchanging methodology a new order of the same test vectors is obtained. The resultant reduction in the hamming distance is depicted in the Table 2.

TABLE II TOTAL HAMMING DISTANCE REDUCTION FOR 3-BIT LFSR

Test Vectors	Test vectors from Conventional LFSR	Reordered Test Vectors
V1	0 1 1	1 0 1
V2	0 0 1	0 0 1
V3	1 0 0	1 0 0
V4	0 1 0	0 1 0
V5	1 0 1	0 1 1
V6	1 1 0	1 1 0
V7	1 1 1	1 1 1
THD	10	9
New order of test vectors: V5→V2→ V3→V4→V1→V6→V7		

V. PROPOSED ARCHITECTURE

Based on the suggested bit interchanging methodology, the modified LFSR can be designed using the conventional LFSR and a group of two-input multiplexers where bit n is considered as the selection line of the multiplexers. The architecture for interchanging the bits as per the proposed methodology is presented in figure 2.

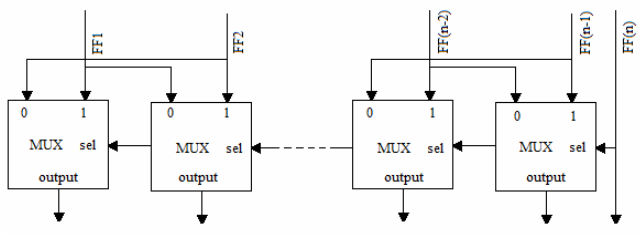

Fig. 2 Architecture of Bit Interchanging Module.

In the figure, a case of odd n is considered. When n is even the interchanging is performed up to third and forth last FF outputs. Embedding the Bit Interchanging Module with the modified clock LFSR makes the design more power efficient as in Figure 3.

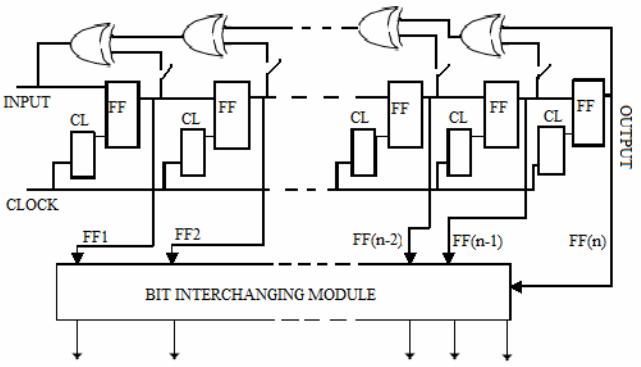

Fig. 3. Proposed general Modified TPG Architecture.

In this architecture the CL block contains the XOR and NOR logic for controlling the clock as shown in Figure. 1. The output from the LFSR is passed to the bit inter-changing module which constitutes of multiplexers. It interchanges the bits as per the proposed methodology and finally generates a set of reordered test vectors.

V.EXPERIMENTS AND ANALYSIS

In order to analyze the power reduction from the proposed TPG architecture, we have evaluated the power consumption in 8 bit conventional LFSR and 8 bit LFSR with modified clock for same input vector and same clock cycles. Experiments were performed Xilinx ISE 9.2i plateform and total power consumption was calculated using Xpower. The result of Table 3, shows that the disabling the flip-flops for a time period when they are not performing, leads to reduction in total power consumption up to 10%.

TABLE III TOTAL POWER CONSUMPTION OF CONVENTIONAL LFSR AND LFSR WITH MODIFIED CLOCK.

LFSR Designs	Total power consumption (mW)
Conventional LFSR	33.59
LFSR with modified clock	30.89

A MATLAB program is written which generates bit-interchanged test vectors. These test vectors are actually the same but their order of scan shifting changes. The THD reduction obtained with maximal length LFSRs is presented in Table 4.

TABLE IV TOTAL HAMMING DISTANCE REDUCTION

Maximal length LFSR	THD without order	THD with order	THD Reduction (%)
4-bit LFSR	31	24	22.58
8-bit LFSR	1014	531	47.63
12-bit LFSR	3517	5649	……
16-bit LFSR	4540	3310	27.09

To predict the power efficiency of the test vectors, Weighted Transition Activity (WTA) was calculated. We used the weighted transition metric (WTM) [7] to predict power consumption due to scan vectors. Power estimation models have been presented in [8]. Consider a scan chain of length l and a scan vector $t_j = t^*_{j,1}\ t^*_{j,2}\ \ldots..\ t^*_{j,k}$ with $t^*_{j,1}$ scanned in before $t^*_{j,2}$ and so on. For n vectors $t_1, t_2, t_3 \ldots.. t_n$ the average power (P_{avg}) is estimated as follows:

$$P_{avg} = \frac{\sum_{j=1}^{n}\sum_{i=1}^{l-1}(l-i).(t^{\bullet}_{j,1} \oplus t^{\bullet}_{j,t+1})}{n} \quad (2)$$

To compare the average power consumption between a conventional LFSR and the Proposed LFSR, we calculated the WTA and thereafter Pavg from the Equation (2). We used test vectors generated from 4bit, 8 bit, 12 bit and 16 bit maximal length LFSRs. The obtained results have been shown in Table 5.

TABLE V COMPARISON OF AVERAGE POWER BETWEEN CONVENTIONAL LFSR AND THE PROPOSED LFSR

LFSR bits	Avg_power (Conventional LFSR)	Avg_power (Proposed LFSR)
4-bits	3.2000	2.7333

8-bits	13.6745	7.4275
12-bits	31.0830	33.4456
16-bits	60.1420	24.7920

The obtained results from Table 5 show the decrease in average power calculated on the basis of weighted transition activity. The reduction in average power depends upon the tap sequences of the maximal length LFSR. Two approaches for indicating the reduction in power consumption *viz.* THD based prediction and WTM based prediction have been used.

VI.CONCLUSION

The proposition is an attempt to invoke research on the test pattern generator itself. The techniques available so far have focused upon reducing the switching activity from the test patterns generated from the generator. Embedding the switching activity minimizing techniques with a power efficient test pattern generators will be a good step ahead. Therefore a modification is proposed in the conventional LFSR by embedding it with control logic module and bit interchanging module. This culminates into a novel architecture of the test pattern generator (TPG). The modified TPG architecture is capable of not only disabling the switching units for a particular time frame but also reorders the test vectors so as to reduce the transition activity. The benefit of the proposed TPG is that it can be used with any other low power technique to have further reduction in power.

REFERENCES

[1] Seongmoon Wang, Sandeep K.Gupta, "ATPG for HEAT Dissipation Minimization During Test Application" *IEEE Trans. On computer* Vol: 47, No. 2, 1998, pp. 256-262.

[2] Abu-Issa, A.S., Quigley, S.F., "Bit Swapping LFSR for low-power BIST", vol.44, Issue 6,401-402,2008.

[3] Mayank Shakya, Soundra Pandian K.K. "Low Power Testing of CMOS Circuits: A Review", proc. of NCSCV'09,vl 106, 2009.

[4] Walter Aloisi and Rosario Mita, Member, IEEE, Gated clock design of Linear Feedback Shift Register , IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS, VOL. 55, NO. 6, JUNE 2008.(references).

[5] P.Girard, C.landrault, S.Pravossoudovitch, D Severac, "Reducing Test power Consumption During Test Vector Ordering" IEEE International Symposium on Circuits and Systems, 1998.

[6] M. Bellos, D. Bakalis, D.Nikolos, X. Kavousianos, "Low Power Testing by vector Ordering with Vector Repetition", pp 205-210,2004.

[7] Artem Sokolov, Alodeep Sanyal, Darrell Whitley, Yashwant Malaiya, "Dynamic Power Minimization During Combinational Circuit Testing as a Traveling Salesman Problem", pp. 1088-1095, 2005.

[8] Anshuman Chandra, Kishendu Chakrabarty, "Low Power Scan Testing and Test Data Compression for a System on Chip", IEEE Transaction on Computer Aided Design of Integrated Circuits and Systems, Vol.21, No.5, May 2002.

[9] K.Paramasivam, K.Gunavathi,"Reordering Algorithm for Minimizing Test Power in VLSI Circuits", Engineering Letter, Issues_v14, February 2007.