Two-dimensional Analytical Drain Current Model for Multilayered-Gate Material Engineered Trapezoidal Recessed Channel (MLGME-TRC) MOSFET: a Novel Design

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Abstract—In this paper, for the first time, a two-dimensional (2D) analytical drain current model for sub-100 nm multi-layered gate material engineered trapezoidal recessed channel (MLGME-TRC) MOSFET: a novel design is presented and investigated using ATLAS and DEVEDIT device simulators, to mitigate the large gate leakages and increased standby power consumption that arise due to continued scaling of SiO2-based gate dielectrics. The two-dimensional (2D) analytical model based on solution of Poisson's equation in cylindrical coordinates,   utilizing the cylindrical approximation, has been developed which evaluate the surface potential, electric field, drain current, switching metric: ION/IOFF ratio and transconductance for the proposed design. A good agreement between the model predictions and device simulation results is obtained, verifying the accuracy of the proposed analytical model.

Keywords—ATLAS, DEVEDIT, NJD, MLGME- TRC MOSFET.

I. INTRODUCTION

STEADY downscaling of device dimensions, innovative device designs and rapid advances in technology are some of the factors that have largely governed the evaluation of CMOS technology at a remarkable rate over the last few decades. As a result denser and faster integrated circuits have been achieved that offer superior performance and much reduced physical size compared to their predecessors. However, the continued miniaturization of MOSFETs in sub-100nm regime, further scaling down of SiO_2 gate dielectric leads to high direct tunneling gate leakage current, which in turn causes increase in device power consumption. To reduce the gate leakage current in small geometry MOSFETs, high-k gate dielectrics emerged as an alternative to conventional SiO2. A high-k gate dielectric layer [1, 2] allows physically thicker films while permitting smaller electrical thickness. It increases the gate control over the channel, but gives rise to unacceptable levels of interface traps [3], bulk fixed charges, low interface carrier mobility and phase instability issues [4]. Thus, it gives way to a gate stacked engineered structure [5, 6] that uses the stack of a thin SiO2 and a thick high-k layer. Thus, an ultra thin SiO2 interlayer between the high-K layer and silicon substrate was introduced (resulting in a multi-layer gate structure) to improve the interface quality and stability. Further, to achieve higher speeds and higher packing densities, gate length miniaturization is the key parameter, but it leads to many SCEs and hot carrier effects.

Multilayered Gate Material Engineered Trapezoidal Recessed Channel (MLGME-TRC) MOSFET design, considered in this study integrates the desired features of multi-layered gate architecture [7,8] such as improvement in gate controllability and reduction in gate leakage and tunneling effects; and those allied with GME-TRC [9] and RC MOSFET [10,11] such as excellent hot carrier immunity, SCE and punchthrough suppression, thereby enhancing the gate controllability over the channel and the electrical and switching characteristics in terms of DIBL, subthreshold swing and hot carrier effects. Thus, multi-layered dielectric gate architecture in conjunction with recessed channel structure is of paramount importance in nanoscale devices which in turn enhances the gate controllability, current driving capabilities, ION/IOFF ratio and transconductance across the channel.

Further, to gain insight into the effectiveness of MLGME-TRC MOSFET design, a simple 2D analytical model has been developed by solving the 2D Poisson equation in cylindrical coordinates, utilizing the cylindrical approximation, and compared with conventional gate material engineered trapezoidal recessed channel (GME-TRC) and trapezoidal recessed channel (TRC) MOSFETs. The device simulators: ATLAS and DEVEDIT [12] have been used to verify the accuracy of the proposed model, and a good agreement between their results is obtained. The proposed design proves its efficacy for improved high performance analog and switching applications.

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World Academy of Science, Engineering and Technology
International Journal of Electronics and Communication Engineering
Vol:4, No:4, 2010

II. MODEL FORMULATION

1. Two dimensional potential and Electric field profile

1.1 Potential analysis:

In the present analysis, the channel region is divided into two parts, since the gate is made up of two different materials laterally merged together. Assuming the concave corner to be part of a cylinder, having radius $r_o = \dfrac{L_p}{2(1+\tan\theta_{o1}/2)}$ [13], Poisson equation in cylindrical coordinates for potential, i.e. $\psi(r,\theta)$, is given by

$$\frac{\partial^2\psi(r,\theta)}{\partial r^2}+\frac{1}{r}\frac{\partial\psi(r,\theta)}{\partial r}+\frac{1}{r^2}\frac{\partial^2\psi(r,\theta)}{\partial\theta^2}=\frac{qN_A}{\varepsilon_{Si}}$$

In the present analysis, the channel region has been divided in to two parts; hence the potential under the gate region M1 and M2 can be represented as

$$\psi_1(r,\theta)=A_{01}(\theta)+A_{11}(\theta)r+A_{21}(\theta)r^2$$

$$for \quad 0\langle\theta\langle\theta_{01} \quad ; \quad r_o+EOT\langle r\langle r_o+EOT+y_d$$

$$\psi_2(r,\theta)=A_{02}(\theta)+A_{12}(\theta)r+A_{22}(\theta)r^2$$

$$for \quad \theta_{01}\langle\theta\langle\theta_{01}+\theta_{02} \quad ; \quad r_o+EOT\langle r\langle r_o+EOT+y_d$$

Where, depletion layer thickness is given by $y_d=\sqrt{\dfrac{2\varepsilon_{Si}}{qN_A}1.5\phi_F}$

And the effective gate oxide thickness, EOT, is given by

$$EOT=t_{ox1}+\frac{\varepsilon_{ox1}}{\varepsilon_{ox2}}t_{ox2},$$

Based on boundary conditions, as shown in Fig.1. the Poisson's equation is solved separately under the two gate regions (M1 and M2) and the potential can be calculated as:

$$\psi_j(r,\theta)=V_{SUB}+\frac{1}{\gamma}\left(\frac{1}{r_o\ln(1+EOT/r_o)}\right).(V_{gj}-\psi_{Sj}(\theta)).$$

$$\left[-\frac{(r_o+EOT+y_d)^2}{2y_d}+\frac{(r_o+EOT+x_d)^2}{y_d}r-\frac{1}{2y_d}r^2\right]$$

where, $j=1,2$ for regions under M1 and M2 respectively.

1.2 Electric field analysis:

The electron velocity through the channel is related to the electric field pattern along the channel. Thus, the electric field is given as

$$E_{Sj}(\theta)=-\frac{d}{r.d\theta}\psi_j(r,\theta)\Big|_{r=r_o+EOT}=-\frac{d}{r.d\theta}\psi_{Sj}(\theta)$$

where, $r=r_o+EOT$

Electric field component, under M1 is given as

$$E_{S1}(\theta)=\frac{1}{r.\lambda\sinh(\theta_{o1}/\lambda)}\{\delta_{11}\cosh((\theta_{o1}-\theta)/\lambda)-\delta_{12}\cosh(\theta/\lambda)\}$$

Electric field component, under M2 is given as

$$E_{S2}(\theta)=\frac{1}{r.\lambda\sinh(\theta_{o2}/\lambda)}.$$

$$\{\delta_{21}\cosh((\theta_{o1}+\theta_{o2}-\theta)/\lambda)-\delta_{22}\cosh((\theta-\theta_{o1})/\lambda)\}$$

2. Drain current and transconductance profile

In this section, I_{ds}-V_{gs} model for the proposed design incorporation with channel length modulation (CLM) effect for linear to saturation region has been summarized [14].

Case.I. linear region

$$I_{ds}=\frac{\mu.C_{oxc}.W}{L_{eff}.\left(1+\dfrac{\delta_o.V_{ds}}{L_{eff}.\varepsilon_c}\right)}.(V_{gs}-V_{th}-0.5.\alpha.V_{ds})$$

Case.II Saturation region

$$I_{ds}=\frac{\mu.C_{oxc}.W}{\left(L_{eff}-l_d\right).\left(1+\dfrac{\delta_o.\mu_s.V_{ds}}{\left(L_{eff}-l_d\right).v_{sat}}\right)}.(V_{gs}-V_{th}-0.5.\alpha.V_{dsx}).V_{dsx}$$

Transconductance:

Transconductance is an important device parameter for analog circuit simulation and can be calculated as:

$$g_m=\frac{\partial I_{ds}}{\partial V_{gs}}\Big|_{V_{ds}=constant}$$

III. RESULT AND DISCUSSION

The schematic structure of MLGME-TRC MOSFET is shown in Fig.1. with metal gates, M1 and M2 of lengths L1 and L2 respectively. In MLGME-TRC MOSFET, the gate consists of multi-layered-gate dielectrics having a thickness t_{ox1} and t_{ox2} of the lower and the upper gate dielectrics with the corresponding permittivites, ε_{ox1} and ε_{ox2}, respectively; and for GME-TRC and TRC MOSFETs: $t_{ox1}=t_{ox2}$.

World Academy of Science, Engineering and Technology
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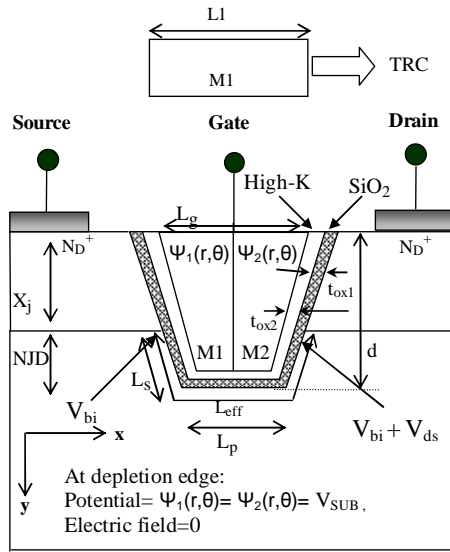
Fig.1.Schematic structure of MLGME-TRC MOSFET, where channel length L_g= L_1 + L_2 =74nm, with work function Φ_{M1}=4.77V and Φ_{M2} = 4.10V for MLGME-TRC and GME-TRC MOSFET and for TRC MOSFET, channel length L_g=L_1=74nm and work function Φ_{M1}=4.77V having Negative junction depth (NJD)=10nm, Groove Depth d=20nm, N_A =1x10^{17} cm^{-3}, N_D=1x10^{20} cm^{-3} , t_{ox1}= t_{ox2} =2nm, L_{eff}=(2 x L_s) + L_p,where L_p=28nm, L_s=14nm unless stated otherwise.

Fig.2. and Fig.3. shows the modeled and simulated results for potential and electric field profile for MLGME-TRC, GME-TRC and TRC MOSFETs. A close proximity between the modeled and simulated results validates the proposed model. Simulation results reveal that TRC-MOSFET with GME architecture improves the device performance with the use of two metal gates i.e. M1(control gate) and M2 (screening gate) where $\Phi M1 > \Phi M2$, in terms of improved gate control and driving current capabilities. This is due to the step in surface potential at the interface of two metals, which results in screening of channel region under metal gate M1 from drain potential variations and hence ensures reduction in DIBL and punch through effects. Further, the significant enhancement in step of potential profile for MLGME-TRC MOSFET, as shown in Fig.2., in comparison with GME-TRC MOSFET is due to improvement in screening effect as a consequence of the incorporation of multi-layered high-K dielectric system that facilitates physically thicker gates, thereby permitting the scaling of gate oxide thickness and thus, increasing gate control over the channel. Fig.3. clearly depicts that for GME-TRC MOSFET, the step in potential forces the electric field to be redistributed on the drain side. This electric field discontinuity at the interface of the two gate metals causes the overall channel field to be more uniform across the channel resulting in the enhancement of carrier transport efficiency across the channel. For, MLGME-TRC MOSFET, the peak in electric field further increases at the interface thereby, improving the current driving capabilities across the channel, due to the improved gate control and hot carrier immunity for ML-GME-TRC MOSFET.
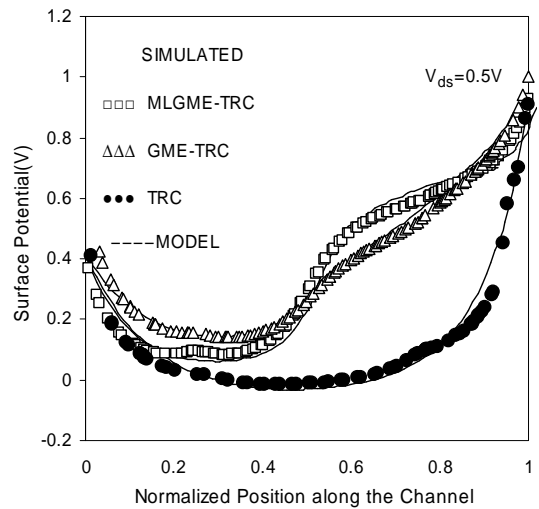

Fig. 2. Potential profile for ML-GME-TRC, GME-TRC and TRC MOSFETs having ε_{ox1}=3.9 and ε_{ox2}=20. The solid line represents the modeled results.
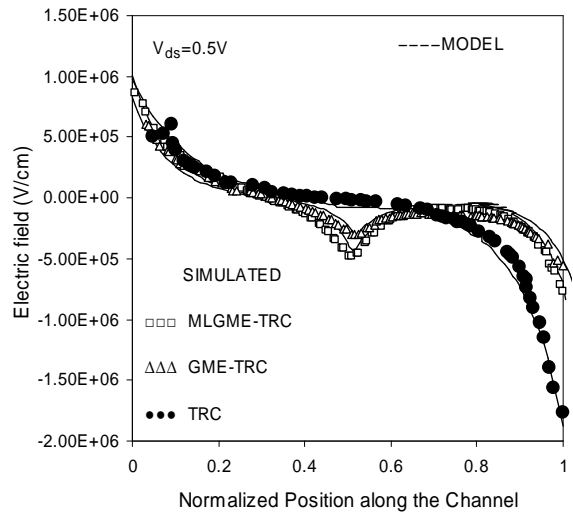

Fig. 3. Electric field profile for ML-GME-TRC, GME-TRC and TRC MOSFETs having ε_{ox1}=3.9 and ε_{ox2}=20. The solid line represents the modeled results.

Fig.4, 5 and 6 shows the drain current, transconductance ION/IOFF ratio profile, respectively, for MLGME-TRC, GME-TRC and TRC MOSFETs. For GME-TRC MOSFET, the step in potential profile results in a more uniform electric field across channel, leading to improved driving current, transconductance, and ION/IOFF ratio as shown in Fig.4, 5 and 6, respectively. The amalgamation of multilayered gate stack and GME-TRC MOSFET, further enhances the peak electric field at the interface, there by improving the drain current and hence the transconductance and switching speed in terms of ION/IOFF ratio as shown in Fig.4, 5 and 6, respectively, due to the improved gate control and; reduces short channel and hot carrier effects for MLGME-TRC MOSFET.

World Academy of Science, Engineering and Technology
International Journal of Electronics and Communication Engineering
Vol:4, No:4, 2010

Fig. 4. Drain to Source current Vs Gate to source Voltage(V_{gs}) for ML-GME-TRC, GME-TRC and TRC MOSFETs having $\varepsilon_{ox1}=3.9$ and $\varepsilon_{ox2}=20$The solid line represents the modeled results.

Fig. 5. Transconductance Vs Gate to source Voltage(V_{gs}) for ML-GME-TRC, GME-TRC and TRC MOSFETs having $\varepsilon_{ox1}=3.9$ and $\varepsilon_{ox2}=20$. The solid line represents the modeled results.

Fig. 6. Simulated I_{ON}/I_{OFF} variation for ML-GME-TRC, GME-TRC and TRC MOSFETs having $\varepsilon_{ox1}=3.9$. The solid line represents the modeled results.

IV. CONCLUSION

In this work, a novel structure, MLGME-TRC MOSFET has been proposed, analyzed and investigated using device simulators: ATLAS and DEVEDIT. Continued scaling of SiO2-based gate dielectrics necessitates the introduction of high-K materials for sub-100 nm technology node. The analytical and simulation results reveal that, MLGME-TRC MOSFET proves to be superior to GME-TRC and TRC MOSFETs in terms of improved gate controllability, enhanced electric field across the channel and thus, increased driving current, transconductance and switching characteristic in terms of ION/IOFF ratio. The proposed MLGME-TRC design, hence, presents its applicability for high speed logic and low standby power (LSP) applications.

ACKNOWLEDGEMENT

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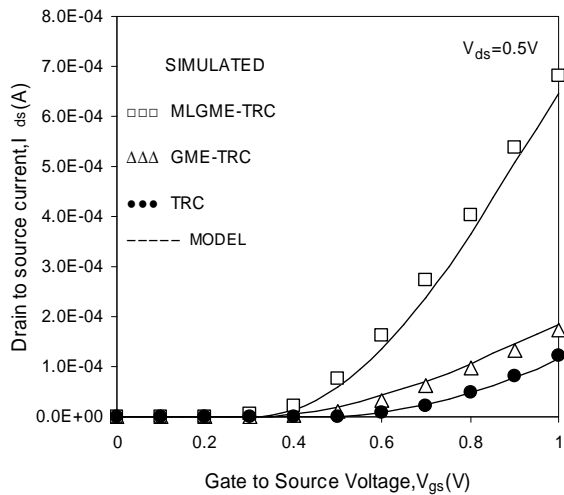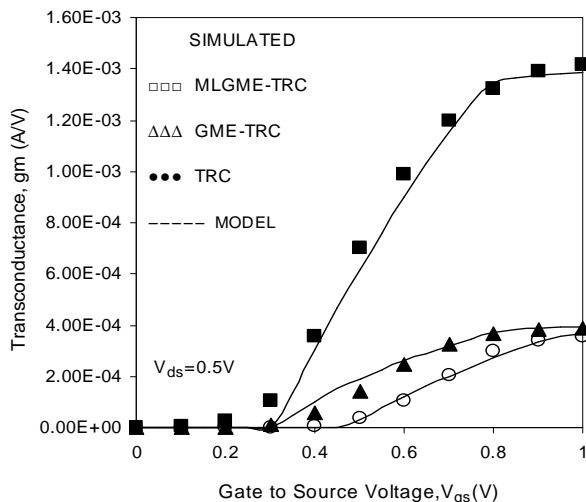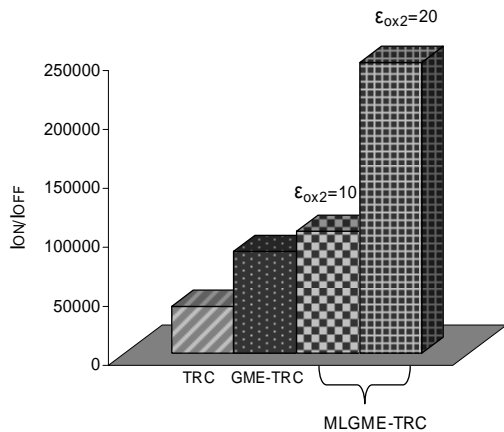[12] ATLAS: 3-D and DEVEDIT: 3D Device Simulator SILVACO International (2002).

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