

# A PWM Controller with Multiple-Access Table Look-up for DC-DC Buck Conversion

Steve Hung-Lung Tu, and Chu-Tse Lee

**Abstract**—A new power regulator controller with multiple-access PID compensator is proposed, which can achieve a minimum memory requirement for fully table look-up. The proposed regulator controller employs hysteresis comparators, an error process unit (EPU) for voltage regulation, a multiple-access PID compensator and a low-power-consumption digital PWM (DPWM). Based on the multiple-access mechanism, the proposed controller can alleviate the penalty of large amount of memory employed for fully table look-up based PID compensator in the applications of power regulation. The proposed controller has been validated with simulation results.

**Keywords**—Multiple access, PID compensator, PWM, Buck conversion.

## I. INTRODUCTION

WITH the proposition of system-on-a-chip (SOC) concept and its applications, built-in power management functions become highly desirable [1]–[3]. Among them, digital power regulator controllers play an important role in the design of dc-dc conversion due to their flexibility, programmability, and low sensitivity to noise interference.

Since the digital controller is used in an inherently analog regulating loop, A/D converters have been also employed in the controller as the interface [4]–[5], in which an n-bit A/D converter can increase the conversion speed and enhance the resolution. However, due to the non-linearity and high-complexity of the delay-line A/D converter, an analog comparator and an EPU were suggested to act as the function of the A/D converter [6], which simply uses the feedback error signal as the input of the EPU state machine to adjust the system output voltage. Due to the inherent simplicity, it may reduce a certain degree of system complexity and of course, power consumption. Moreover, a fully table look-up approach for the controller were proposed in [5], in which the operation results of the PID compensator and the DPWM were pre-calculated and stored in a memory. The input data to the compensator is treated as the address to access the memory and the memory output is a 1-MHz clock signal with variable duty cycle. The approach can take advantages of the memory usage in a SOC system due to their regular operation characteristic.

According to the report in [5], however the direct implementation of the approach can lead to a problem in the memory requirements.

In this paper, we propose a multiple-access mechanism to achieve a minimum memory requirement for fully table look-up based PID compensators. In turn, a fully table look-up based controller can be proposed, which is especially suitable for SOC implementation.

## II. THE PROPOSED REGULATOR ARCHITECTURE

The proposed regulator controller is shown in Fig. 1, which comprises two analog comparators with and without hysteresis characteristic, an EPU, a multiple-access table look-up based PID compensator and a DPWM.  $V_{ref}$  is the reference voltage employed to compare with the regulated output voltage  $v_{out}(t)$  and yields a 2-bit *Error\_voltage* bus with four possible binary values 2'b00 / 2'b01 / 2'b10 / 2'b11 from the comparators. The output of the *Error\_voltage* bus is sent to the EPU which develops an error signal  $e(n)$  ranging from  $-4$  to  $+4$  to represent the output regulated voltage tuning range  $-(\Delta v_{out})_{max}/2$  to  $+(\Delta v_{out})_{max}/2$  [4].  $V_q$  is defined as the resolution of the output regulated voltage, which is equal to  $(\Delta v_{out})_{max}/8$ . The compensated signal  $d(n)$  is ranging from 1 to 254. The DPWM develops *Duty(t)* which is a signal of 1 MHz with  $d(n)/256$  duty cycle. According to *Duty(t)* and all internal parameters, the converter develops the regulated output voltage  $v_{out}(t)$  and the operation of the controller iterates until  $v_{out}(t)$  is equal to  $V_{ref}$ .

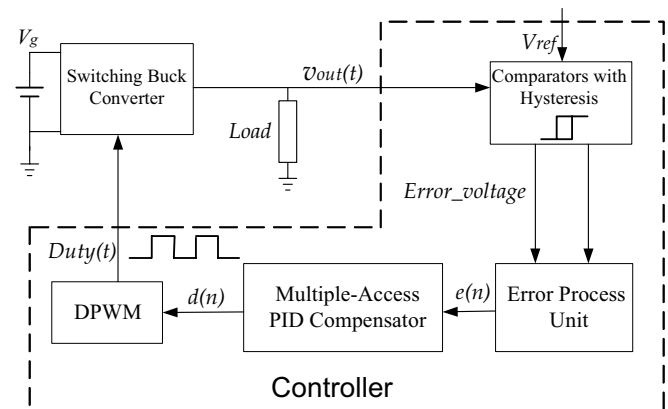


Fig.1. Block diagram of the proposed dc-dc regulator controller.  
A. EPU (Error Process Unit) -

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Fig. 2 illustrates the EPU state transition diagram. The mechanism of the proposed EPU can be described as follows. Assuming an iterative signal  $v_{out}(t)$  is required to trace another signal  $V_{ref}$  and let *Error\_voltage* be the output of the comparators, whose value can be described as follows

$$\begin{aligned} \text{Error\_voltage} &= 2^{\cdot}b00 && \text{if } V_{ref}-v_{out}(t) \leq -V_q \\ &= 2^{\cdot}b11 && \text{if } V_{ref}-v_{out}(t) \geq V_q \\ &= 2^{\cdot}b01/2^{\cdot}b10 && \text{if } |V_{ref}-v_{out}(t)| < V_q \end{aligned} \quad (1)$$

$e(n)$  is thus the output of the EPU, which indicates the present state of the EPU state machine and it is also proportional to the difference of  $V_{ref}$  and  $v_{out}(t)$ .

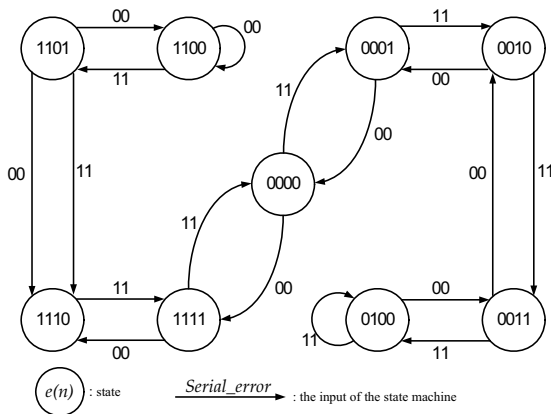


Fig.2. State transition diagram of the EPU.

As the controller starts to iterate, the EPU state machine comes to work depending on the 2-bit input signal *Error\_voltage* from the comparators. If the input signal is  $2^{\cdot}b11$ , then  $e(n)=e(n-1)+1$ , else if the input signal is 00,  $e(n)=e(n-1)-1$ , otherwise  $e(n)=e(n-1)$ . Obviously, it can be implemented with a 4-bit register to cover the range from -4 to +4. Table I shows the state transition table of the EPU.

TABLE I  
 STATE TRANSITION TABLE OF THE EPU

Present state	Next state											
	<i>Serial_error=00</i>				<i>Serial_error=11</i>				<i>Serial_error=01/10</i>			
Q3 Q2 Q1 Q0	D3 D2 D1 D0	D3 D2 D1 D0	D3 D2 D1 D0	D3 D2 D1 D0	D3 D2 D1 D0	D3 D2 D1 D0	D3 D2 D1 D0	D3 D2 D1 D0	D3 D2 D1 D0	D3 D2 D1 D0	D3 D2 D1 D0	
0 1 0 0 (4)	0 0 1 1 (3)	0 1 0 0 (4)	0 1 0 0 (4)	0 1 0 0 (4)	0 1 0 0 (4)	0 1 0 0 (4)	0 1 0 0 (4)	0 1 0 0 (4)	0 1 0 0 (4)	0 1 0 0 (4)	0 1 0 0 (4)	
0 0 1 1 (3)	0 0 1 0 (2)	0 1 0 0 (4)	0 1 0 0 (4)	0 0 1 1 (3)	0 0 1 1 (3)	0 0 1 1 (3)	0 0 1 1 (3)	0 0 1 1 (3)	0 0 1 1 (3)	0 0 1 1 (3)	0 0 1 1 (3)	
0 0 1 0 (2)	0 0 0 1 (1)	0 0 1 1 (3)	0 0 1 1 (3)	0 0 1 0 (2)	0 0 1 0 (2)	0 0 1 0 (2)	0 0 1 0 (2)	0 0 1 0 (2)	0 0 1 0 (2)	0 0 1 0 (2)	0 0 1 0 (2)	
0 0 0 1 (1)	0 0 0 0 (0)	0 0 1 0 (2)	0 0 1 0 (2)	0 0 0 1 (1)	0 0 0 1 (1)	0 0 0 1 (1)	0 0 0 1 (1)	0 0 0 1 (1)	0 0 0 1 (1)	0 0 0 1 (1)	0 0 0 1 (1)	
0 0 0 0 (0)	1 1 1 1 (-1)	0 0 0 1 (1)	0 0 0 1 (1)	0 0 0 0 (0)	0 0 0 0 (0)	0 0 0 0 (0)	0 0 0 0 (0)	0 0 0 0 (0)	0 0 0 0 (0)	0 0 0 0 (0)	0 0 0 0 (0)	
1 1 1 1 (-1)	1 1 1 0 (-2)	0 0 0 0 (0)	0 0 0 0 (0)	1 1 1 1 (-1)	1 1 1 1 (-1)	1 1 1 1 (-1)	1 1 1 1 (-1)	1 1 1 1 (-1)	1 1 1 1 (-1)	1 1 1 1 (-1)	1 1 1 1 (-1)	
1 1 1 0 (-2)	1 1 0 1 (-3)	1 1 1 1 (-1)	1 1 1 1 (-1)	1 1 1 0 (-2)	1 1 1 0 (-2)	1 1 1 0 (-2)	1 1 1 0 (-2)	1 1 1 0 (-2)	1 1 1 0 (-2)	1 1 1 0 (-2)	1 1 1 0 (-2)	
1 1 0 1 (-3)	1 1 1 0 (-4)	1 1 1 0 (-2)	1 1 1 0 (-2)	1 1 0 1 (-3)	1 1 0 1 (-3)	1 1 0 1 (-3)	1 1 0 1 (-3)	1 1 0 1 (-3)	1 1 0 1 (-3)	1 1 0 1 (-3)	1 1 0 1 (-3)	
1 1 0 0 (-4)	1 1 1 0 (-4)	1 1 0 1 (-3)	1 1 0 1 (-3)	1 1 0 0 (-4)	1 1 0 0 (-4)	1 1 0 0 (-4)	1 1 0 0 (-4)	1 1 0 0 (-4)	1 1 0 0 (-4)	1 1 0 0 (-4)	1 1 0 0 (-4)	

B. PID Compensator –

The most general control law of the table look-up based

architecture performs the following discrete-time PID control law [7],

$$d(n) = d(n-1) + a \cdot e(n) + b \cdot e(n-1) + c \cdot e(n-2) \quad (2)$$

which indicates that the new compensated value,  $d(n)$ , can be computed with the past compensated value,  $d(n-1)$ , and the new and past values of the error signal,  $e(n)$ ,  $e(n-1)$ , and  $e(n-2)$ . Since  $a, b, c$  are constants, the products  $(a \cdot e)$ ,  $(b \cdot e)$  and  $(c \cdot e)$  can be implemented with look-up table  $a$ , table  $b$  and table  $c$ , respectively. Note that except memories for the look-up tables, we also need three 8-bit adders to compute equation (2). An alternative approach is being the employment of more memories to achieve “fully table look-up” [5], in which a  $2^{20} \times 8$  memory is required to implement the table directly.

However, due to the correlation between the three consecutive error signals  $e[n]$ ,  $e[n-1]$ , and  $e[n-2]$  of the EPU state machine, the totally 12-bit address can be only have 71 possibilities, which can greatly reduce the memory requirement. The ‘multiple-access’ mechanism which the table look-up computation can be executed with different stages under the embedded timing as shown in Fig. 3, in which the operation comprises three stages (i) to (iii) and we also require a 4-MHz clock signal where

$$e'(n) \equiv a \cdot e(n) + b \cdot e(n-1) + c \cdot e(n-2) \quad (3)$$

$$d(n) \equiv d(n-1) + e'(n) \quad (4)$$

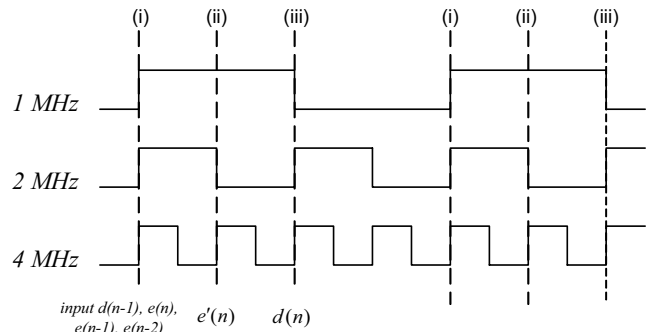


Fig. 3. Operating timing waveforms of the proposed multiple-access mechanism for fully table look-up PID compensator.

In other words, we firstly latch the input data  $d(n-1)$ ,  $e(n)$ ,  $e(n-1)$ , and  $e(n-2)$ . At stage (ii), we use the 12-bit address ( $e(n)$ ,  $e(n-1)$ ,  $e(n-2)$ ) to retrieve 4-bit memory data as the result of  $a \cdot e(n) + b \cdot e(n-1) + c \cdot e(n-2)$ . Note that the 71 possible permutations only lead to less than 16 possible  $e'(n)$ , which can be coded with 4-bit data. Finally, at stage(iii) we use the retrieved 4-bit  $e'(n)$  and 8-bit  $d(n-1)$  as the address to retrieve another memory and obtain  $d(n)$ , which finishes the table look-up operation. Fig. 4 shows the block diagram of the multiple-access PID compensator.

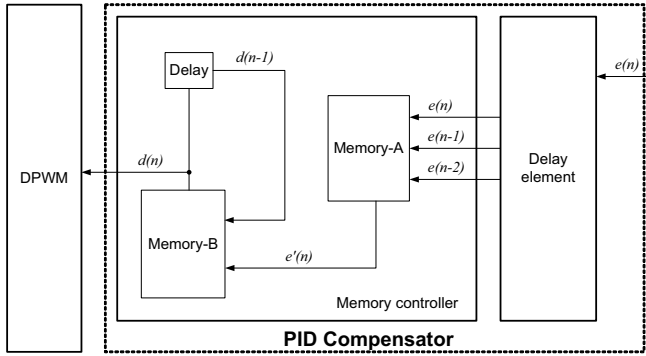


Fig.4. Block diagram of the multiple-access table look-up based PID compensator.

### C. DPWM –

The DPWM employed in this paper is based on a hybrid multi-phase/counter approach, which the concept of low-power dissipation is similar to the design described in [4], [8]. Fig. 5 shows the block diagram of the DPWM.

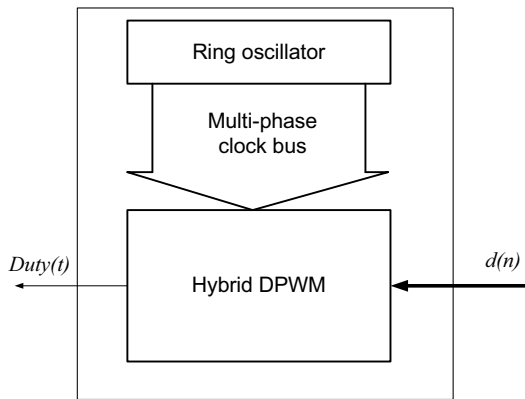


Fig. 5. Block diagram of the DPWM with an embedded ring oscillator.

The multi-phase clock source is generated from an embedded ring oscillator. Note that if the regulator is a functional block in an SOC system, the clock source can be from a differential VCO of the embedded phase-locked loop (PLL), which can provide even more accurate timing leading to more accurate duty ratio.

## III. SIMULATION RESULTS

The system simulation has been performed with SIMULINK. Fig.6 shows the simulation model and the simulation condition is: the input voltage  $V_g = 3.3V$ , the output voltage is regulated at  $v_{out} = 1.8V$ , the load resistor  $R_{load} = 18\Omega$ ,  $L = 98\mu H$ ,  $C = 125nF$ , in which  $L$  and  $C$  are employed in the switching buck converter as shown in Fig.7. The parameters of the PID compensator are:  $a = 12.5$ ,  $b = -23.5$ ,  $c = 11.5$  and the sum of equation (2) can be calculated with the Euler's method [9]. Note that the sum can be pre-calculated and stored the values in an external memory.

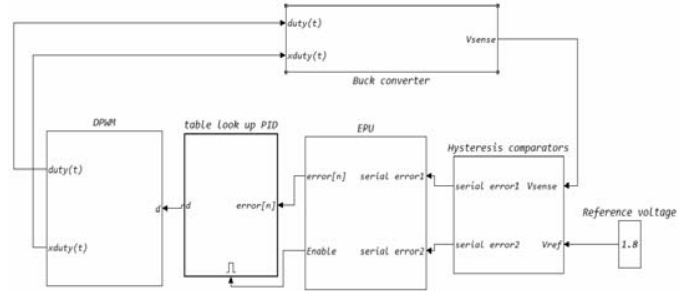


Fig.6. Simulation model of the regulator in SIMULINK.

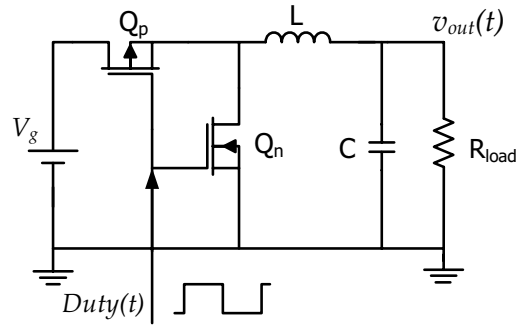


Fig.7. Schematic of the switching buck converter.

Fig.8 shows the steady-state operating waveforms. Obviously, the EPU state  $e(n)$  keeps constant at the steady state and also different  $d(n)$  value is corresponding to different pulse-width signal  $Duty(t)$ .

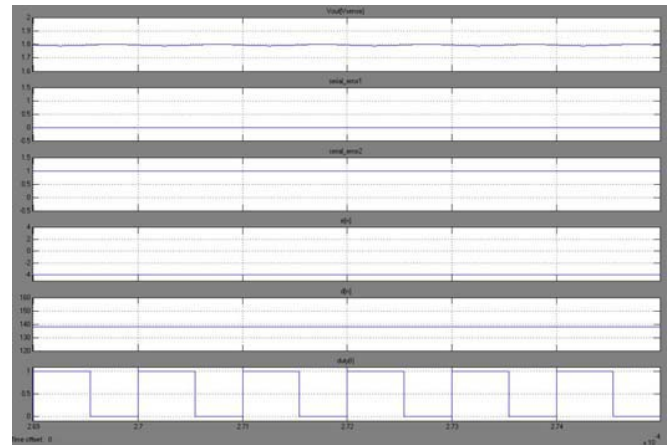


Fig. 8. Steady-state operating waveforms.

Fig.9 shows the load transient response from 100mA to 200mA (load is from  $18\Omega$  to  $9\Omega$ ). The upper waveform is the regulated output voltage and the lower waveform is the load current. Fig. 10(a) indicates the line transient response for the case of  $V_g$  from 3.3V to 4V. The upper waveform is the regulated output voltage. The line transient response for the case of  $V_g$  from 3.3V to 2.6V is shown in Fig. 10(b), where the upper waveform is the regulated output voltage.

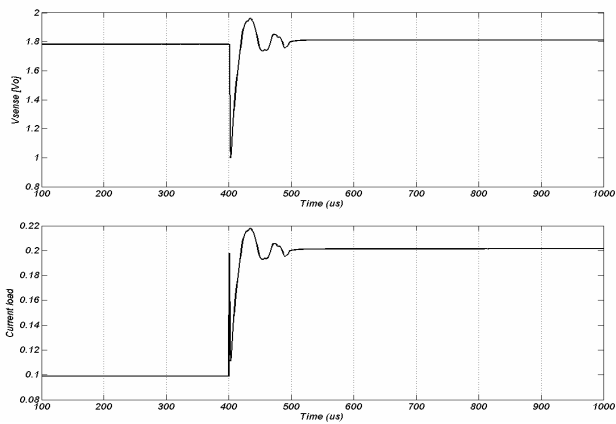


Fig.9. Waveforms of  $v_{out}(t)$  and  $i_{out}(t)$  for the load transient response.

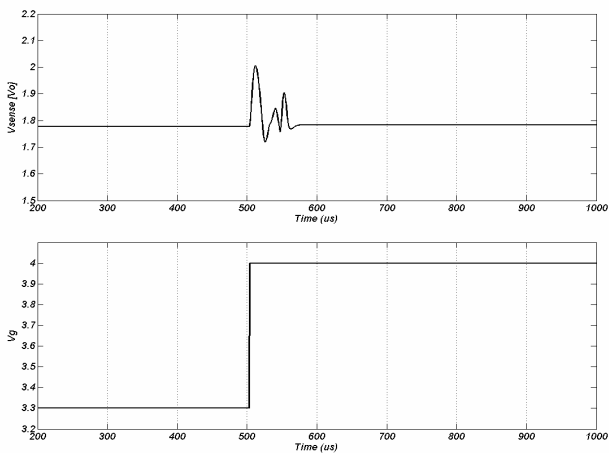


Fig.10(a). Waveform of  $v_{out}(t)$  for line transient response ( $V_g$  from 3.3V to 4V).

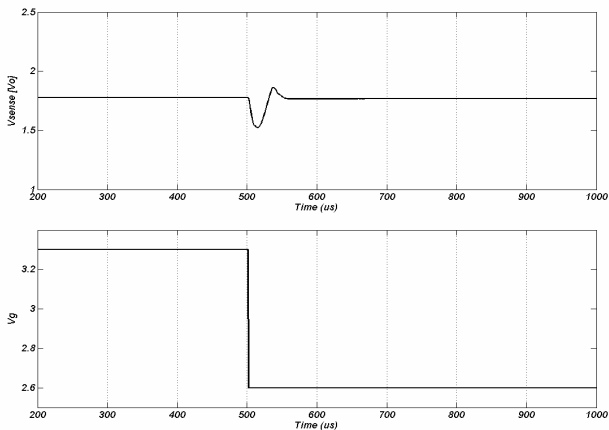


Fig.10(b). Waveform of  $v_{out}(t)$  for line transient response ( $V_g$  from 3.3V to 2.6V).

The simulated waveform of power-up transient period is shown in Fig. 11. Obviously the convergent time is approximately  $90\mu s$ .

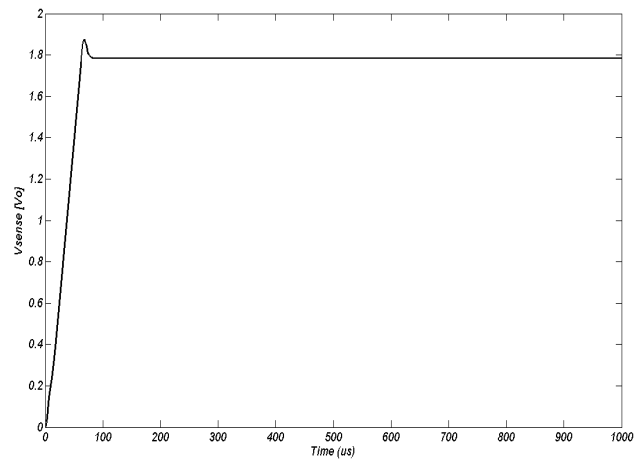


Fig.11. Waveform of  $v_{out}(t)$  at the power-up transient.

#### IV. CONCLUSION

This paper describes a novel DPWM regulator controller based on the proposed multiple-access mechanism. The employment of comparators with hysteresis can stabilize the EPU state transition. Furthermore, the EPU state machine, DPWM, and multiple-access table look-up based PID compensator can be implemented with hardware description language (HDL) and external-access RAM's, which are suitable for single-chip SOC realization.

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